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MSI:MS-7245

NEC:(Babel)(MT3H)

Version 0C

System Chipset:

Intel Broadwater - GMCH (North Bridge)

Intel ICH8(DO)(R) (South Bridge)

On Board Chipset:

BIOS -- SPI Flash 8Mb or 16Mb

HD AUDIO -- ALC262

LPC Super I/O -- SMSC--SHC5017

LAN -- Intel Neneveh 82566 DM/DC

IDE-- VIA VT-6410

CLOCK -- CY505YC64CT

Main Memory:

2 CHANNEL DDR II * 4 (Max 8GB)

Expansion Slots:

PCIE x16 SLOT * 1

PCIE x1 SLOT * 1

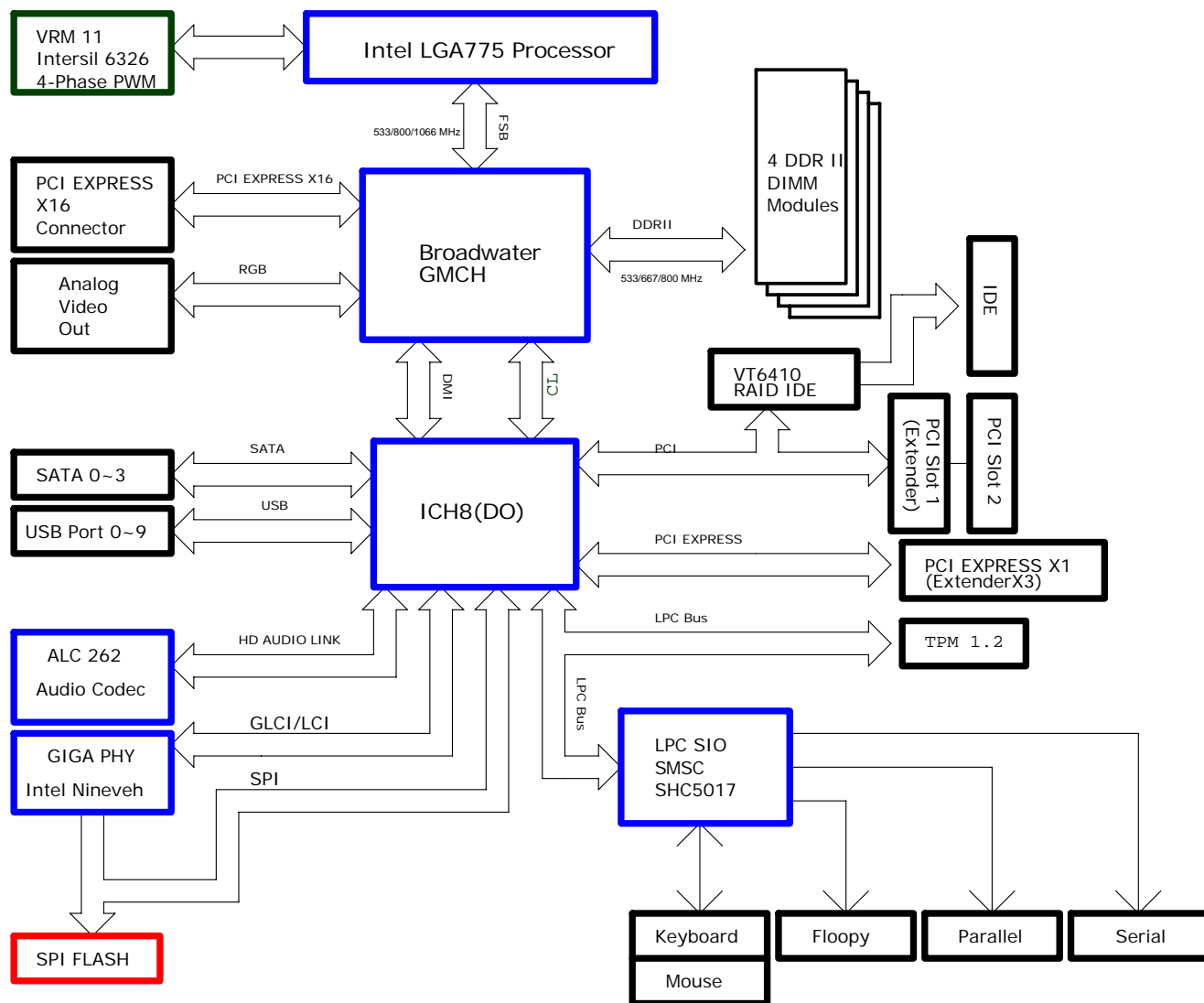
PCI SLOT * 1

PCI(Extender)SLOT * 1

Intersil PWM:

Controller: INTERSIL 6326 4 PHASES

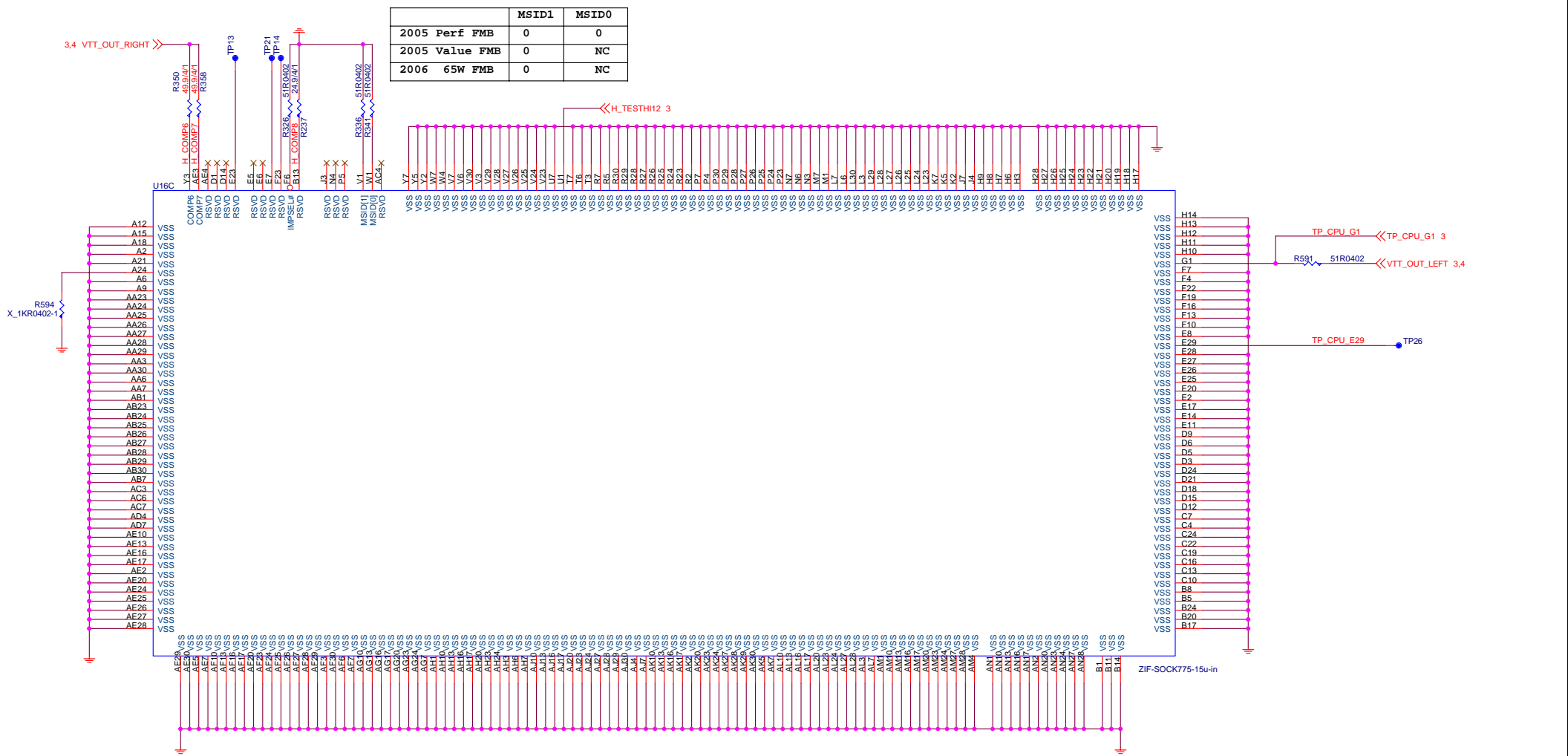
Block Diagram



[illegible]

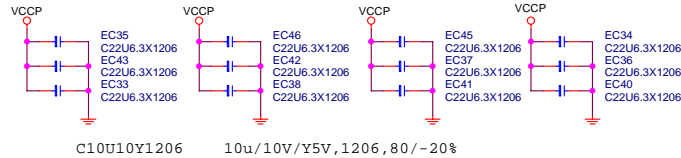
BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)

CPU_TMPA_AR75 0R0402 ↔ CPU_TMPA_SST 16
VTIN_GND_C R78 0R0402 ↔ VTIN_GND_SST 16
CPU_TMPA_AR76 X 0R0402 ↔ CPU_TMPA 24
VTIN_GND_C R79 X 0R0402 ↔ VTIN_GND 24

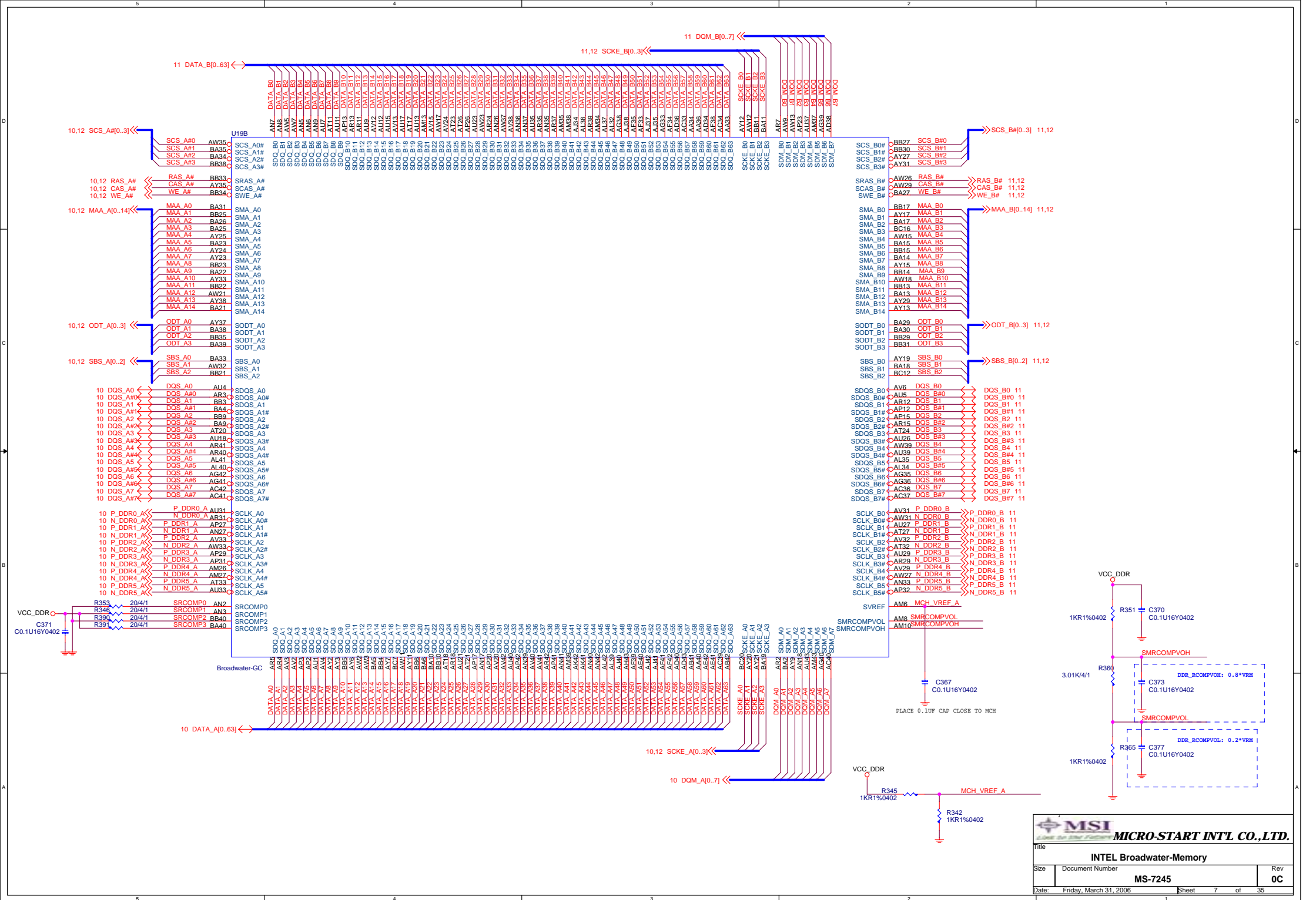


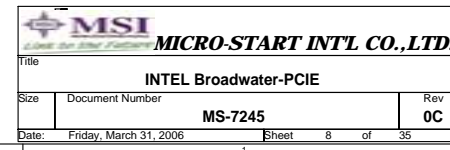
	MSID1	MSID0
2005 Perf FMB	0	0
2005 Value FMB	0	NC
2006 65W FMB	0	NC

CPU DECOUPLING CAPACITORS

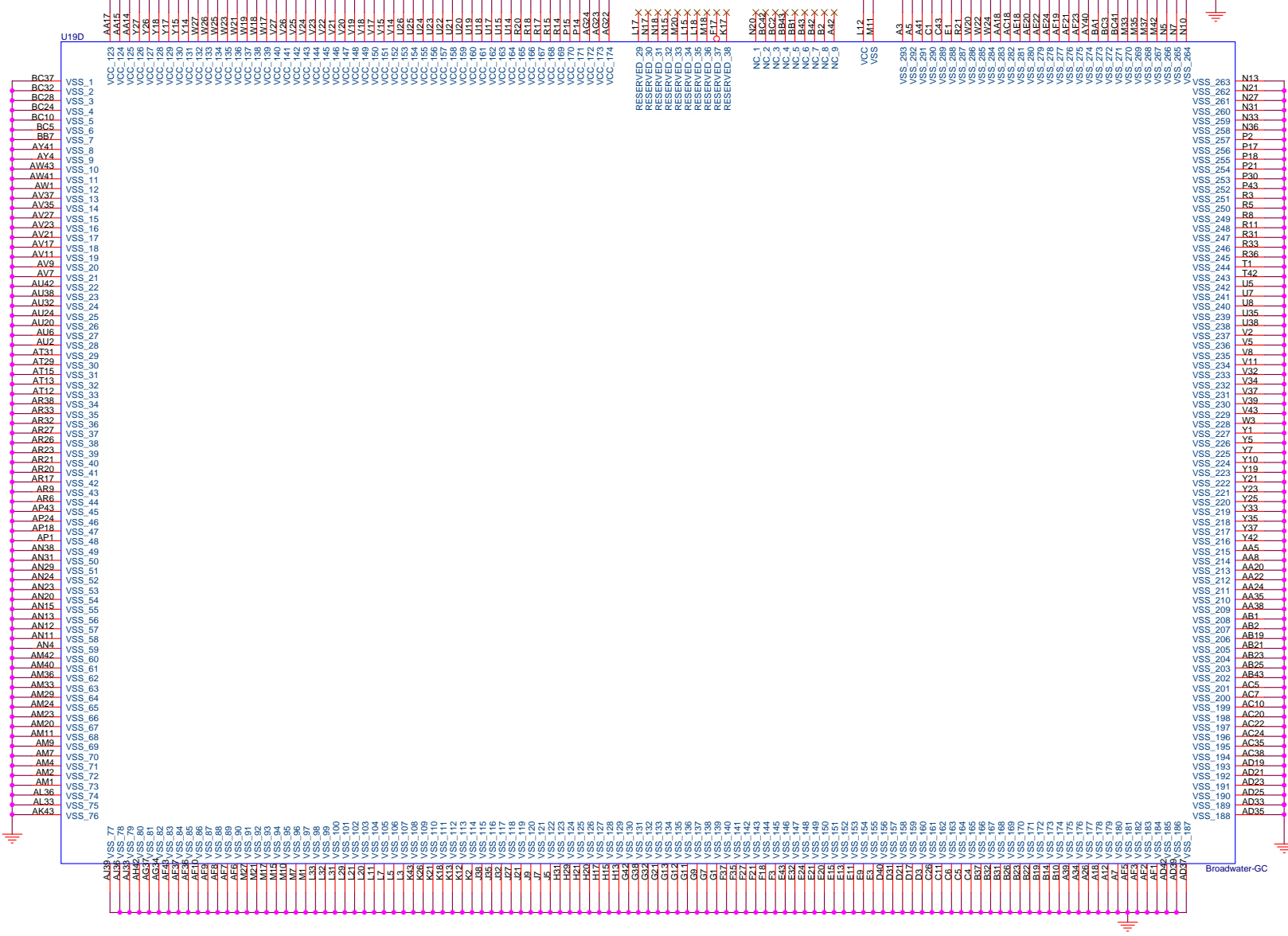



Place these caps within socket cavity





V_1P25_CORE



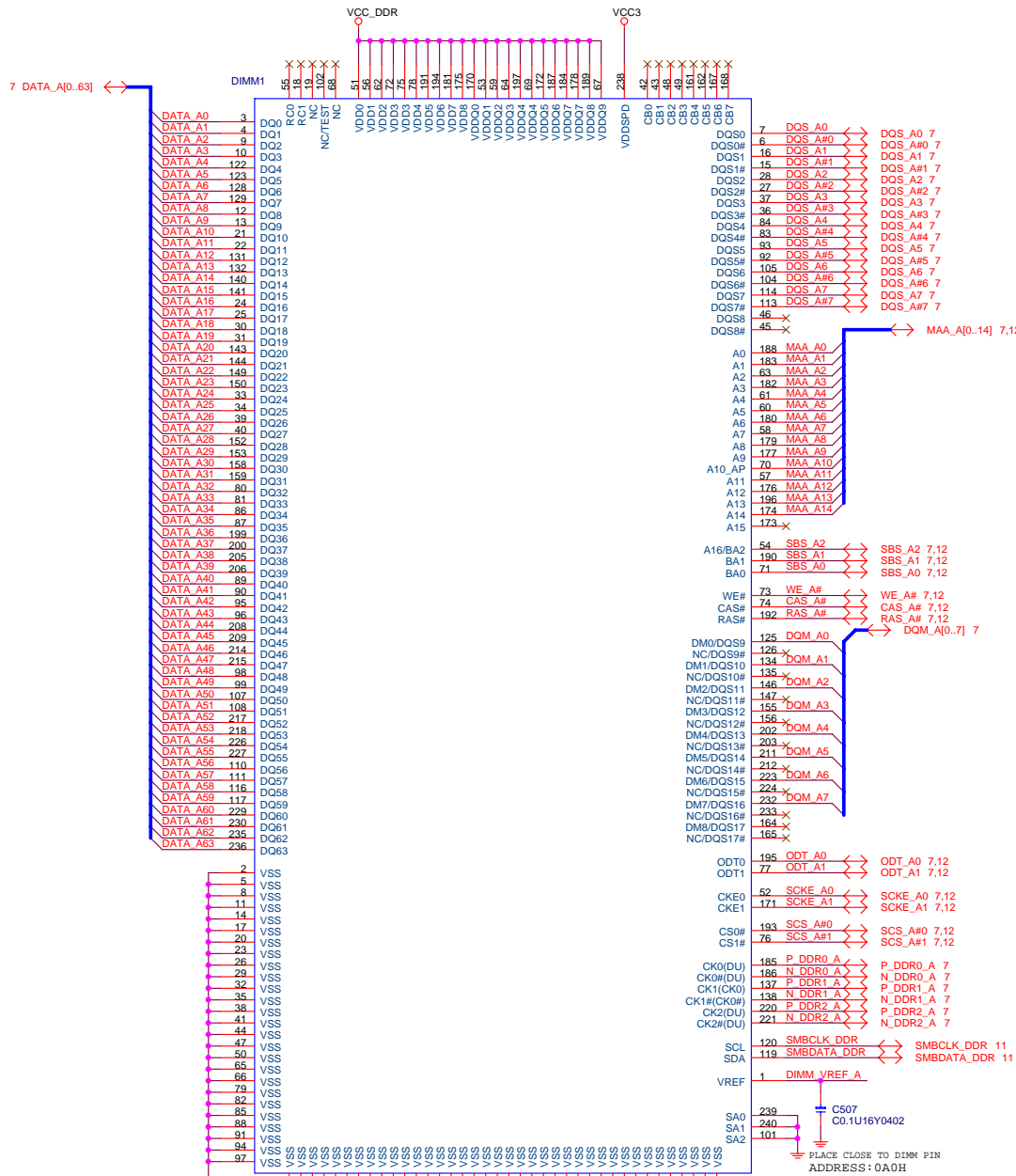


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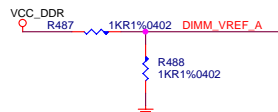
Title

INTEL Broadwater-GND

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[Close to Channel A Dimm]



DDR2 DIMM1

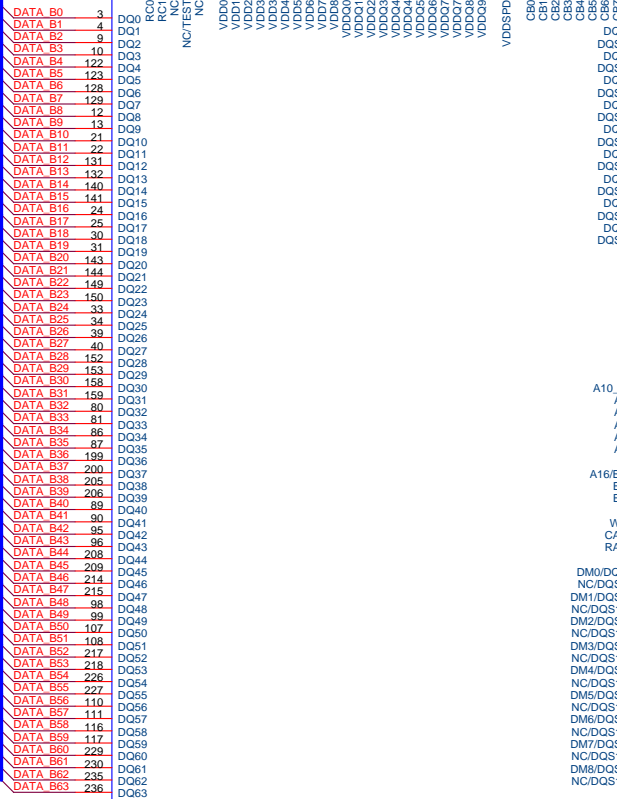
SMBCLK_DDR R529 33R0402-2 SMBCLK_ISO 18,24,27

SMBDATA_DDR R528 33R0402-2 SMBDATA_ISO 18,24,27

DDR2 DIMM2

7 DATA_B[0..63]

DIMM3



DIMM3

DIMM3

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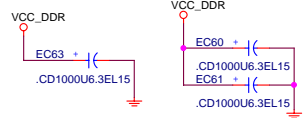
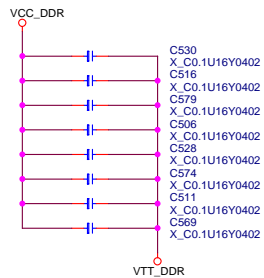
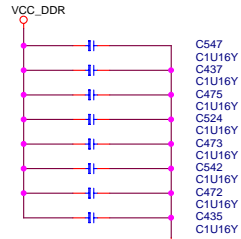
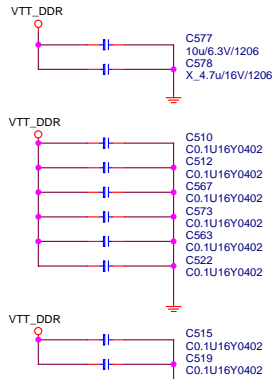
DIMM3

DIMM3

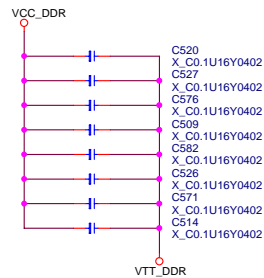
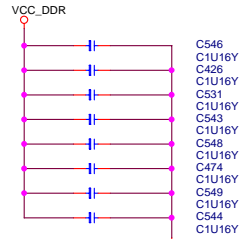
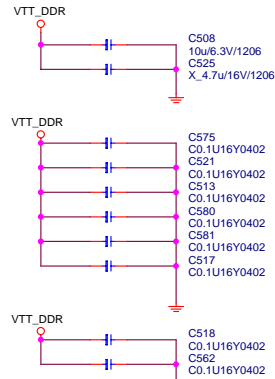
DIMM3

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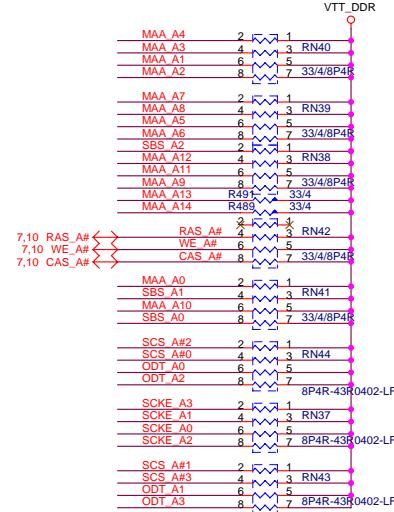
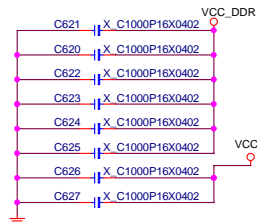
CHANNEL A V_SM_VTT DECOUPLING CAPS



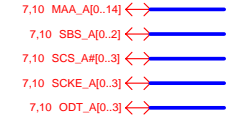
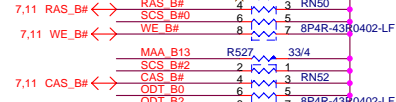
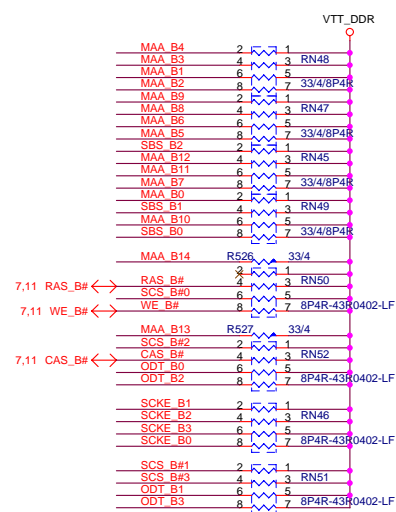
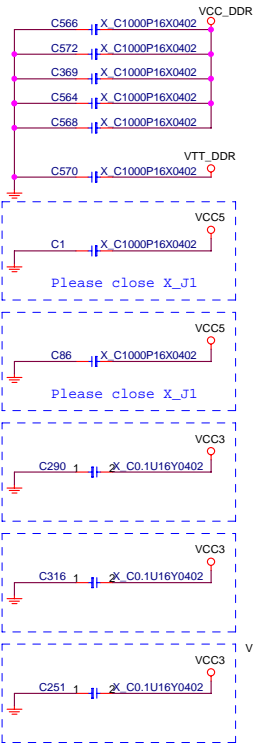
CHANNEL B V_SM_VTT DECOUPLING CAPS



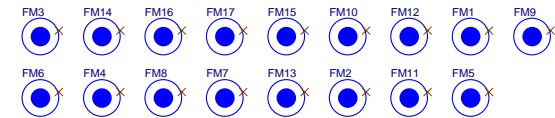
EMI CAPS reserve



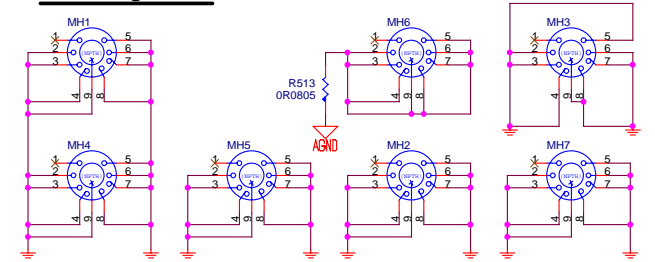
EMI CAPS reserve



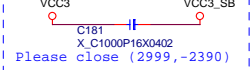
Optical Fiducial Marks



Mounting Holes

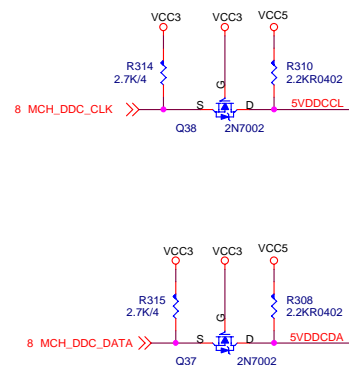
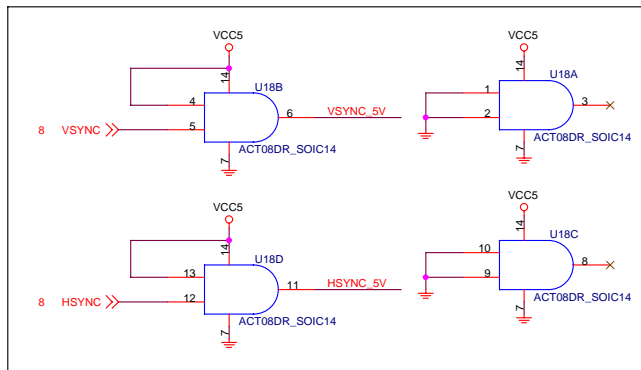
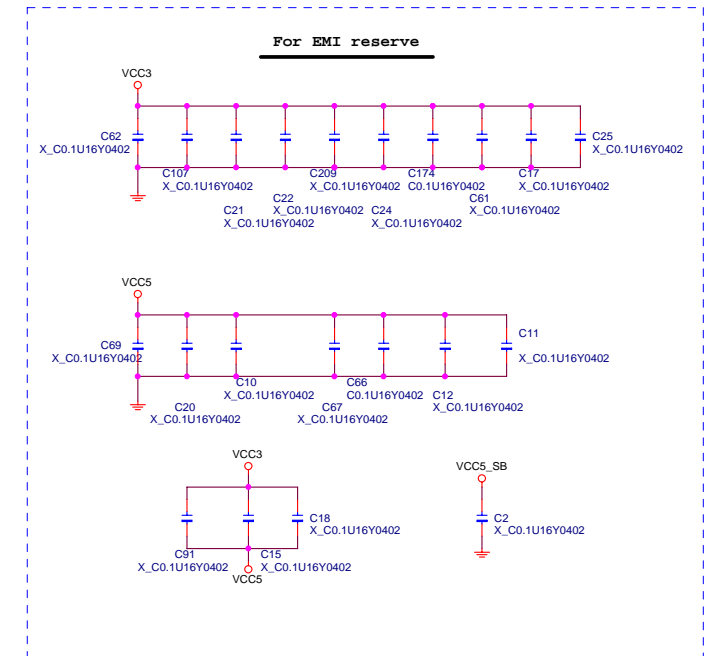
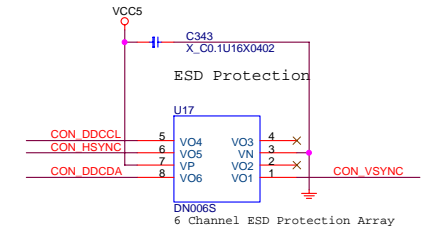
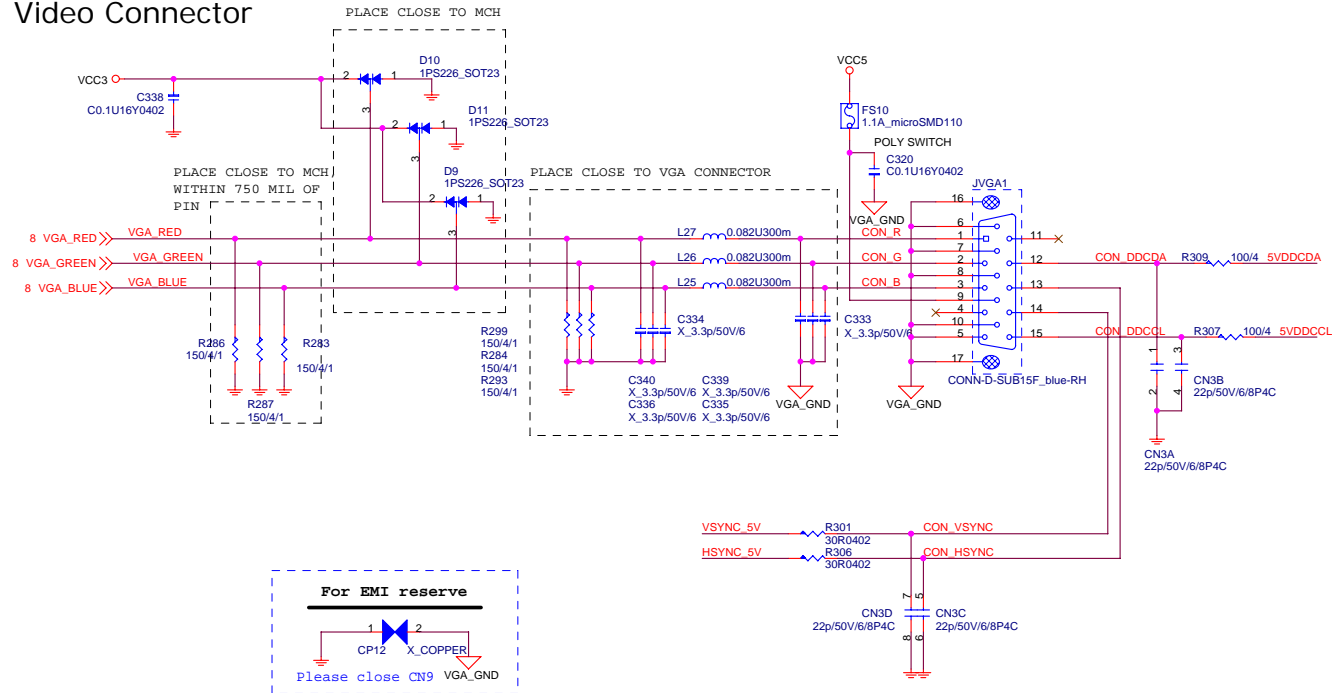



For EMI reserve

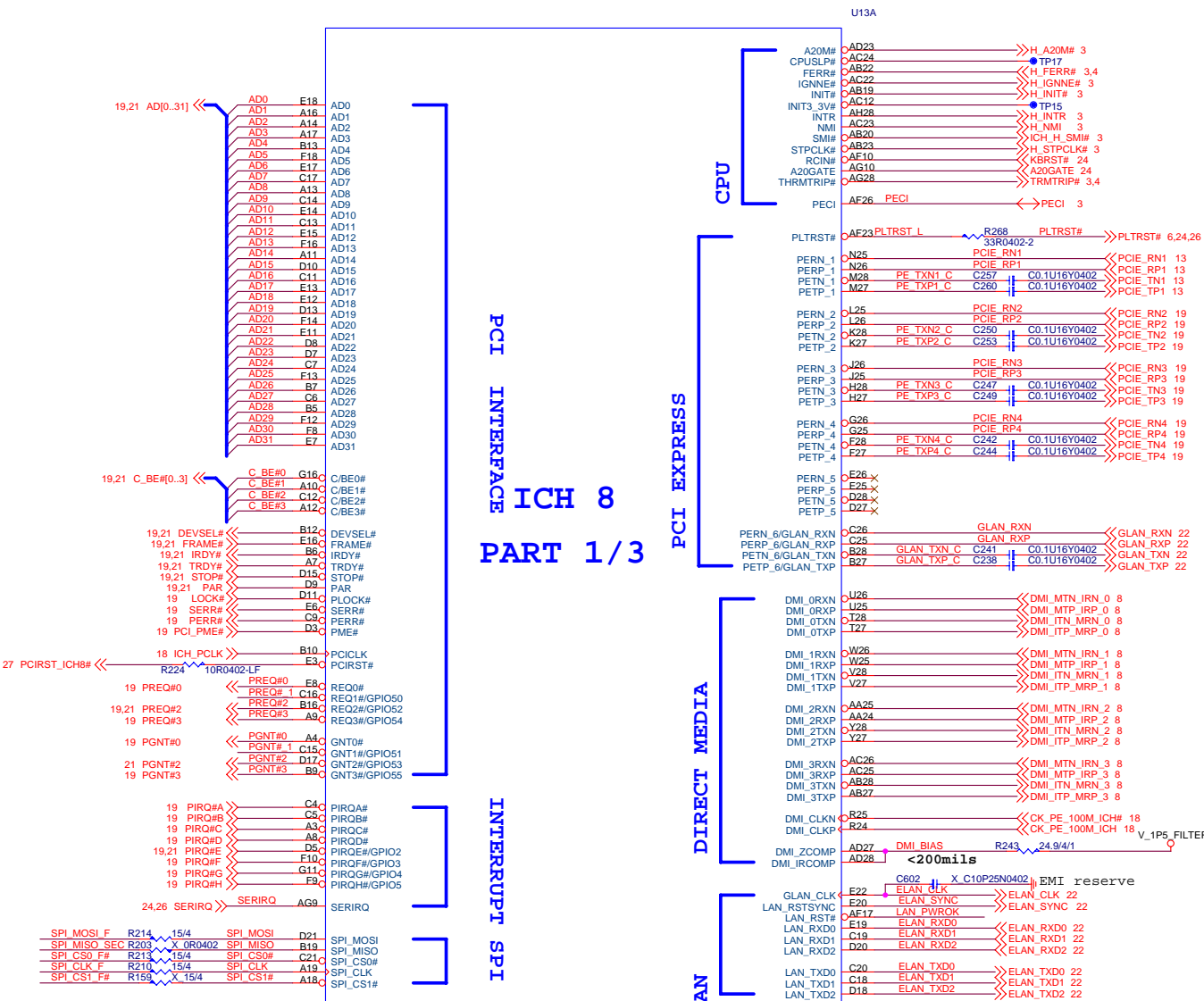


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Title		
DDR TERMINATION		
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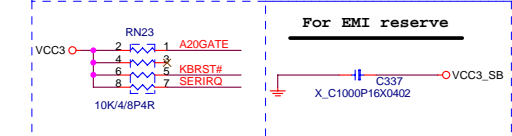
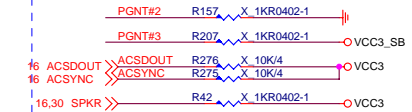
Video Connector



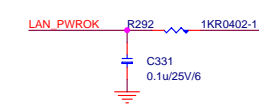
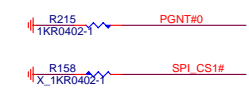
 MICRO-START INTL CO.,LTD.		
Title		
VGA CONNECTOR		
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ICH8 H/W STRAPS			
SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERRIDE
INTVRMEN	EN	DIS	INT VRM
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	DFX/PCIE	N/A	XOR MODE/PCIE PORT CONFIG
HDA_SYNC	SET BIT	N/A	PCIE PORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG BIT 0 (5-6)

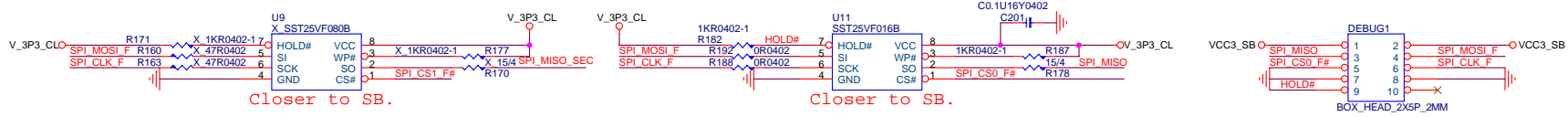


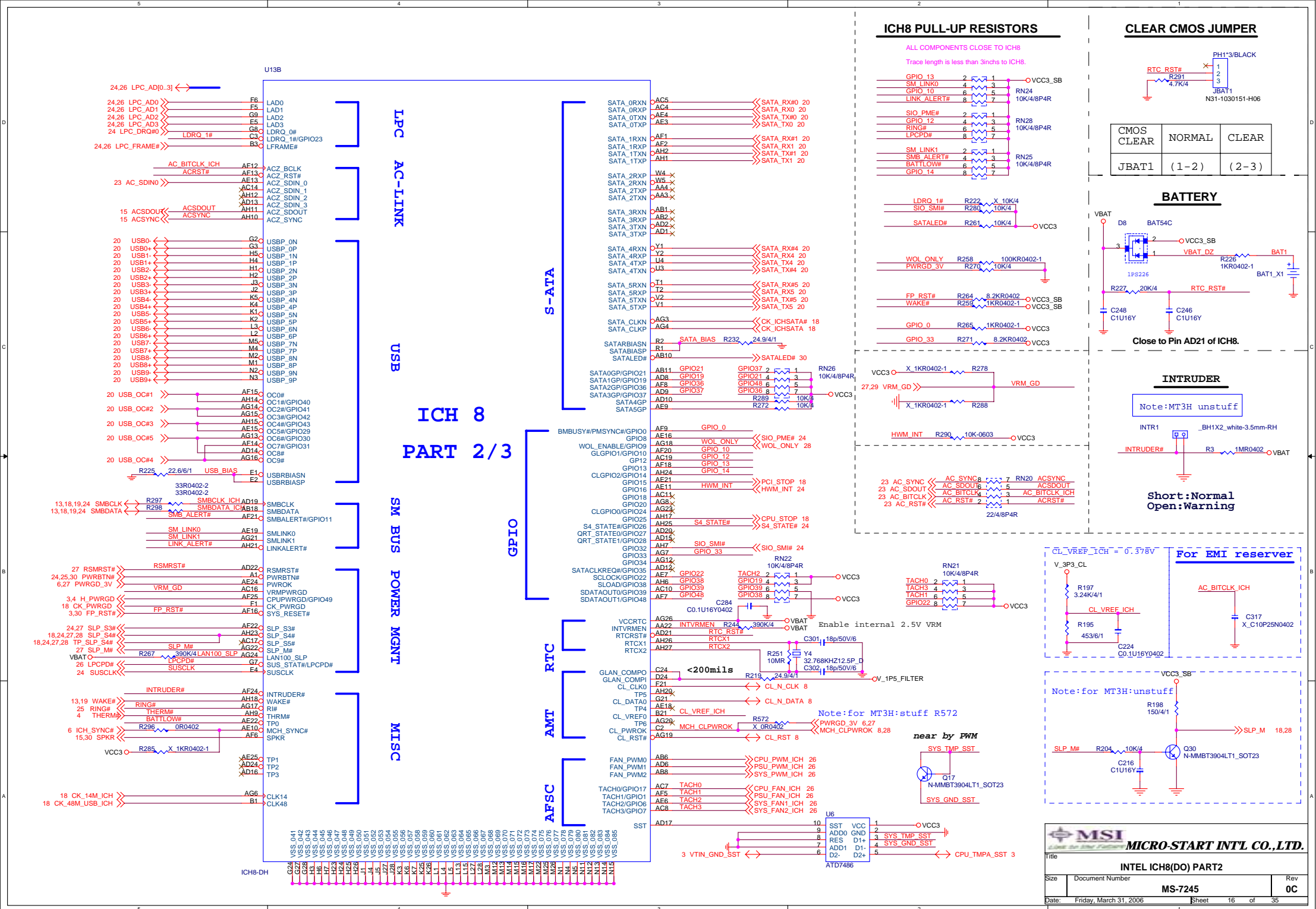
BOOT SELECT STRAPS			
BOOT DEVICE	GNT0	SPI_CS1#	JBOOT1
FWH	1	1	1-2
SPI	0	X	2-3(Default)
PCI	1	0	1-2 & R158



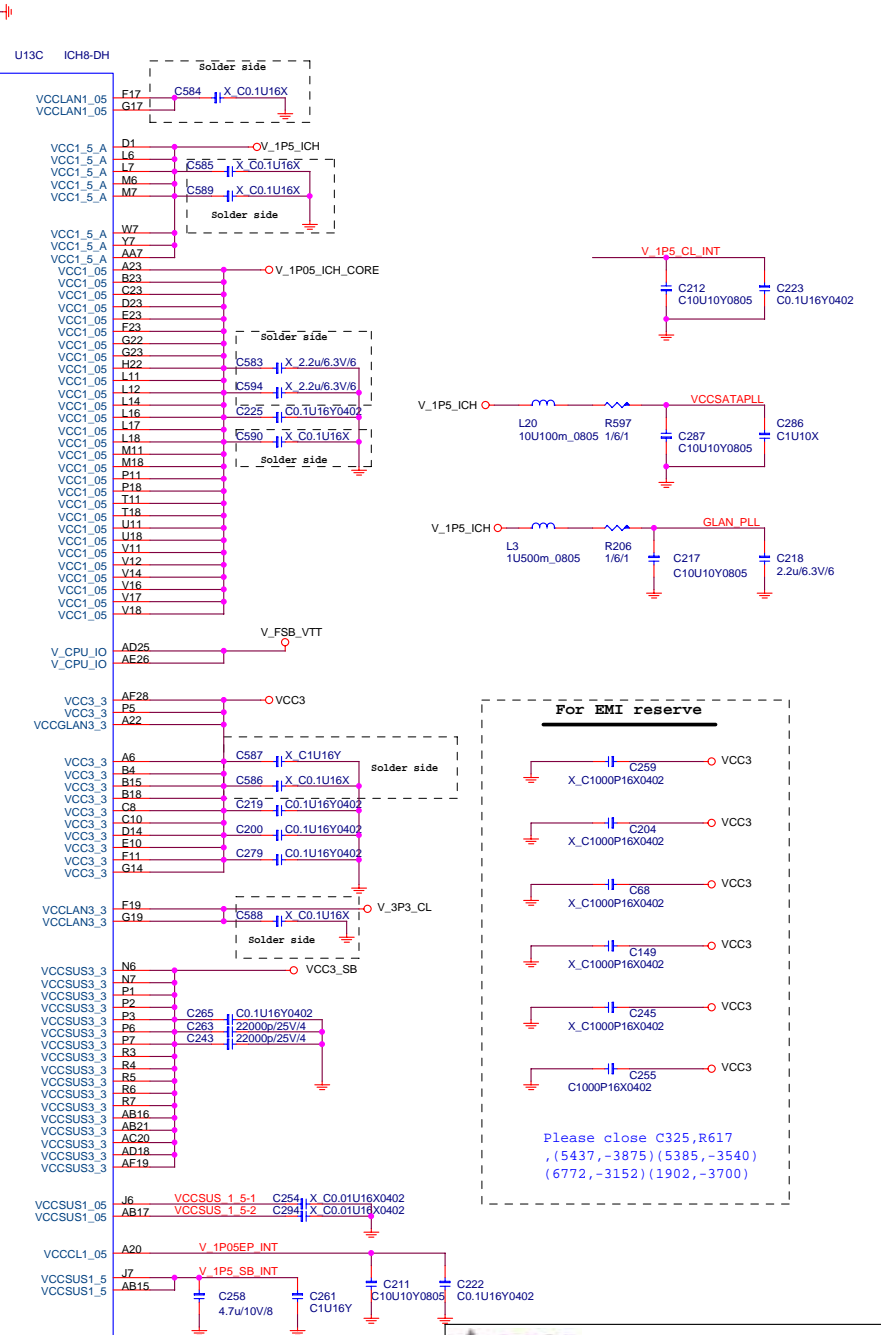
STD: R211, R209 Mount, R199, R208 unmount
For NEC daughter card: R199, R208 Mount
R211, R209 Remove

SPI Debug Port





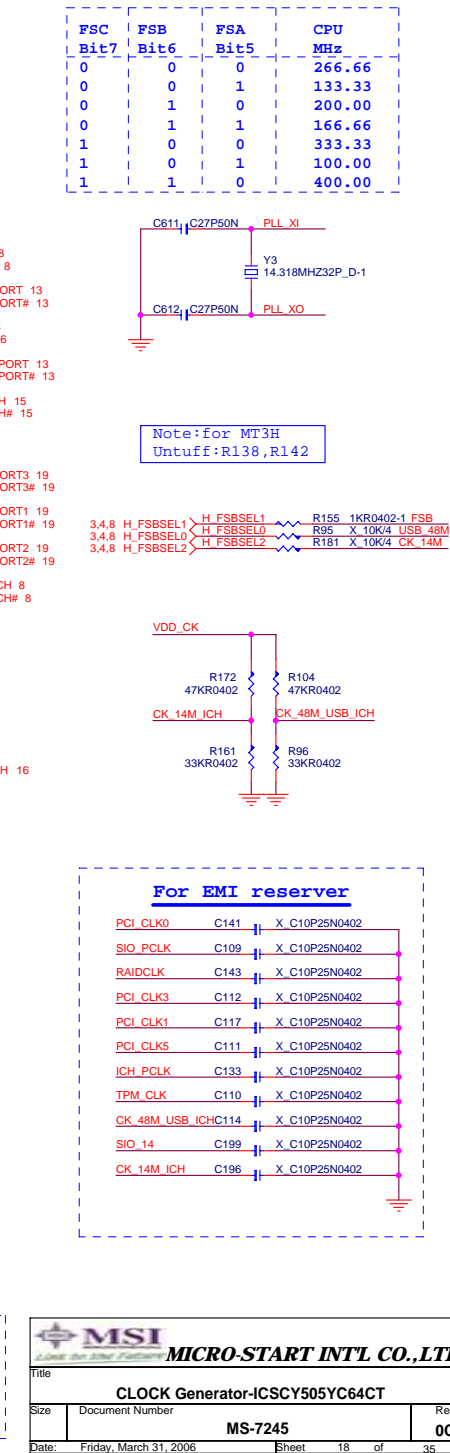
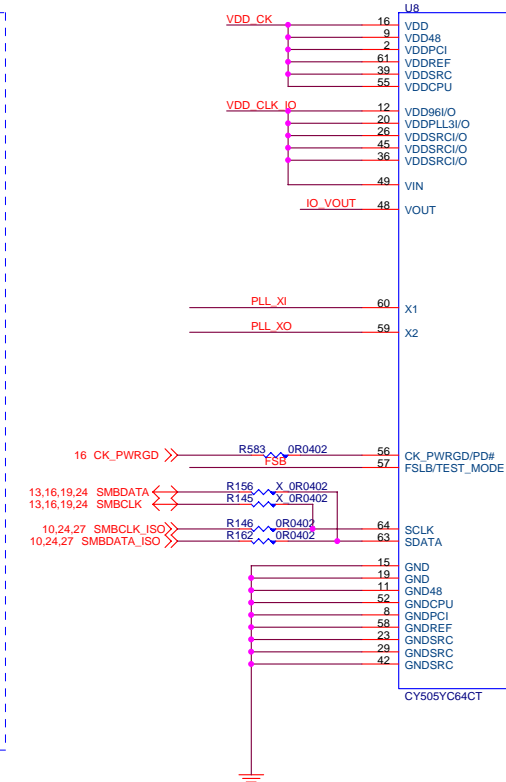
V26	VSS_134	VSS_085	N16
V25	VSS_135	VSS_087	N17
W27	VSS_136	VSS_088	N18
V2	VSS_137	VSS_089	N28
V3	VSS_138	VSS_091	P12
V4	VSS_139	VSS_092	P13
V5	VSS_140	VSS_093	P15
AA2	VSS_141	VSS_094	P16
AA3	VSS_142	VSS_095	P17
AA4	VSS_143	VSS_096	P27
AB1	VSS_144	VSS_097	P27
AB2	VSS_145	VSS_098	R11
AB3	VSS_146	VSS_100	R13
AB4	VSS_147	VSS_101	R14
AC1	VSS_148	VSS_102	R15
AC2	VSS_149	VSS_103	R16
AC3	VSS_150	VSS_104	R17
AC4	VSS_151	VSS_105	R18
AC5	VSS_152	VSS_106	T3
AC6	VSS_153	VSS_107	T5
AD3	VSS_155	VSS_108	T6
AD5	VSS_156	VSS_109	T6
AD7	VSS_157	VSS_110	T6
AD8	VSS_158	VSS_111	T12
AD9	VSS_159	VSS_112	T14
AE1	VSS_160	VSS_113	T14
AE2	VSS_161	VSS_114	T15
AE3	VSS_162	VSS_115	T16
AE4	VSS_163	VSS_116	T22
AE5	VSS_164	VSS_117	T22
AE6	VSS_165	VSS_118	T26
AE7	VSS_166	VSS_119	U1
AE8	VSS_167	VSS_120	U2
AE9	VSS_168	VSS_121	U2
AF1	VSS_170	VSS_122	U12
AG1	VSS_171	VSS_123	U14
AG2	VSS_172	VSS_124	U15
AG3	VSS_173	VSS_125	U16
AG4	VSS_174	VSS_126	U16
AH3	VSS_175	VSS_127	U27
AH4	VSS_176	VSS_128	U28
AH5	VSS_177	VSS_129	V7
AH6	VSS_178	VSS_130	V8
AH7	VSS_179	VSS_131	V18
AH8	VSS_180	VSS_132	V22
AH9	VSS_181	VSS_133	V22
G5	VSS		
AH8	VSS_ICHDET		
AF2	VSSKUMBG		
F1	VSSAUBG		
B2	VSSASATABG		
B22	VSSAIGBG		
V26	VSS_134	VCC1_05	VCC1_5_A
W27	VSS_136	VCC1_05	VCC1_5_A
V2	VSS_137	VCC1_05	VCC1_5_A
V3	VSS_138	VCC1_05	VCC1_5_A
V4	VSS_139	VCC1_05	VCC1_5_A
V5	VSS_140	VCC1_05	VCC1_5_A
AA2	VSS_141	VCC1_05	VCC1_5_A
AA3	VSS_142	VCC1_05	VCC1_5_A
AA4	VSS_143	VCC1_05	VCC1_5_A
AB1	VSS_144	VCC1_05	VCC1_5_A
AB2	VSS_145	VCC1_05	VCC1_5_A
AB3	VSS_146	VCC1_05	VCC1_5_A
AB4	VSS_147	VCC1_05	VCC1_5_A
AC1	VSS_148	VCC1_05	VCC1_5_A
AC2	VSS_149	VCC1_05	VCC1_5_A
AC3	VSS_150	VCC1_05	VCC1_5_A
AC4	VSS_151	VCC1_05	VCC1_5_A
AC5	VSS_152	VCC1_05	VCC1_5_A
AC6	VSS_153	VCC1_05	VCC1_5_A
AD3	VSS_155	VCC1_05	VCC1_5_A
AD5	VSS_156	VCC1_05	VCC1_5_A
AD7	VSS_157	VCC1_05	VCC1_5_A
AD8	VSS_158	VCC1_05	VCC1_5_A
AD9	VSS_159	VCC1_05	VCC1_5_A
AE1	VSS_163	VCC1_05	VCC1_5_A
AE2	VSS_164	VCC1_05	VCC1_5_A
AE3	VSS_165	VCC1_05	VCC1_5_A
AE4	VSS_166	VCC1_05	VCC1_5_A
AE5	VSS_167	VCC1_05	VCC1_5_A
AE6	VSS_168	VCC1_05	VCC1_5_A
AE7	VSS_169	VCC1_05	VCC1_5_A
AE8	VSS_170	VCC1_05	VCC1_5_A
AE9	VSS_171	VCC1_05	VCC1_5_A
AG1	VSS_172	VCC1_05	VCC1_5_A
AG2	VSS_173	VCC1_05	VCC1_5_A
AG3	VSS_174	VCC1_05	VCC1_5_A
AG4	VSS_175	VCC1_05	VCC1_5_A
AH3	VSS_176	VCC1_05	VCC1_5_A
AH4	VSS_177	VCC1_05	VCC1_5_A
AH5	VSS_178	VCC1_05	VCC1_5_A
AH6	VSS_179	VCC1_05	VCC1_5_A
AH7	VSS_180	VCC1_05	VCC1_5_A
AH8	VSS_181	VCC1_05	VCC1_5_A
G5	VSS	VCC1_05	VCC1_5_A
AH8	VSS_ICHDET	VCC1_05	VCC1_5_A
AF2	VSSKUMBG	VCC1_05	VCC1_5_A
F1	VSSAUBG	VCC1_05	VCC1_5_A
B2	VSSASATABG	VCC1_05	VCC1_5_A
B			

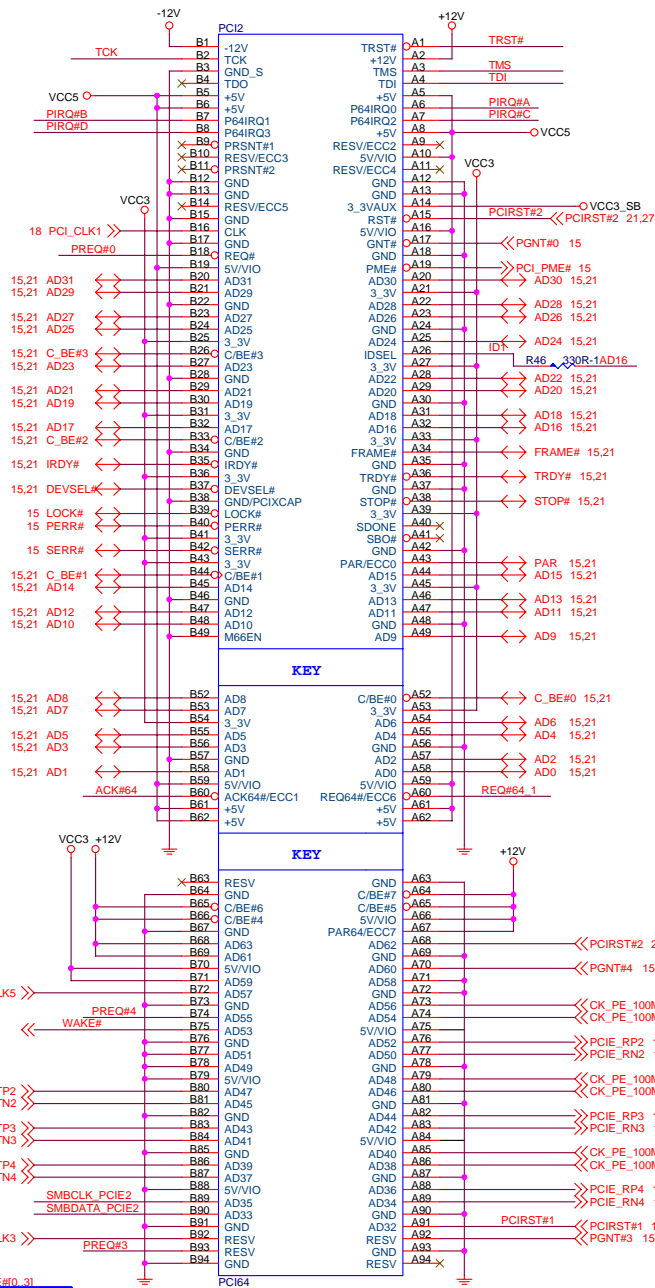


```

Please put all caps close CLK GEN.

```



PCI1/PCIEXTENT

IDSEL = AD16

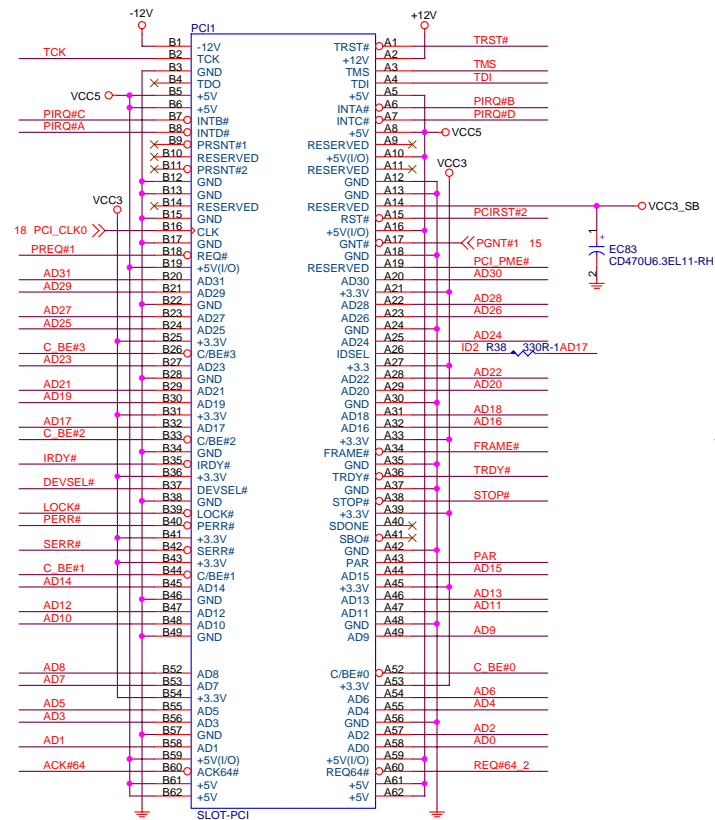
MASTER = PREQ#0
PIRQ#A

PCI3 RESERVE

```

IDSEL = AD18
MASTER = PREQ#3
PIRQ#C

```

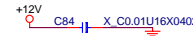
PCI SLOT 2 (PCI VER: 2.3 COMPLY)

IDSEL = AD17

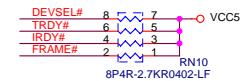
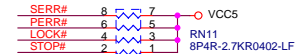
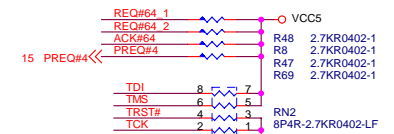
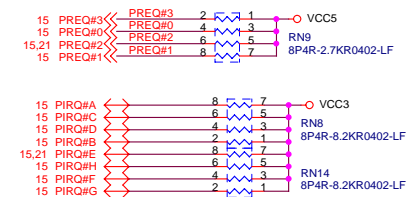
MASTER = PREQ#1

PIRQ#B

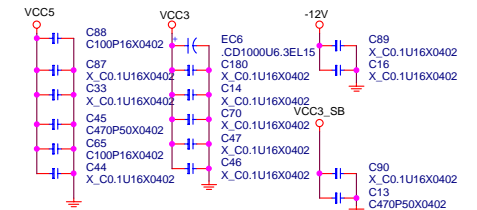
For EMI reserve



PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



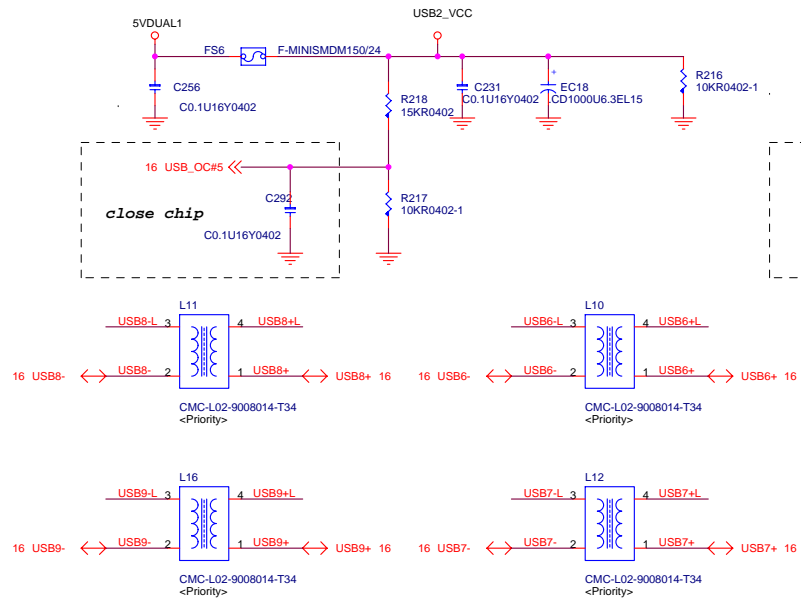
MICRO-START INT'L CO., LTD.

Title	
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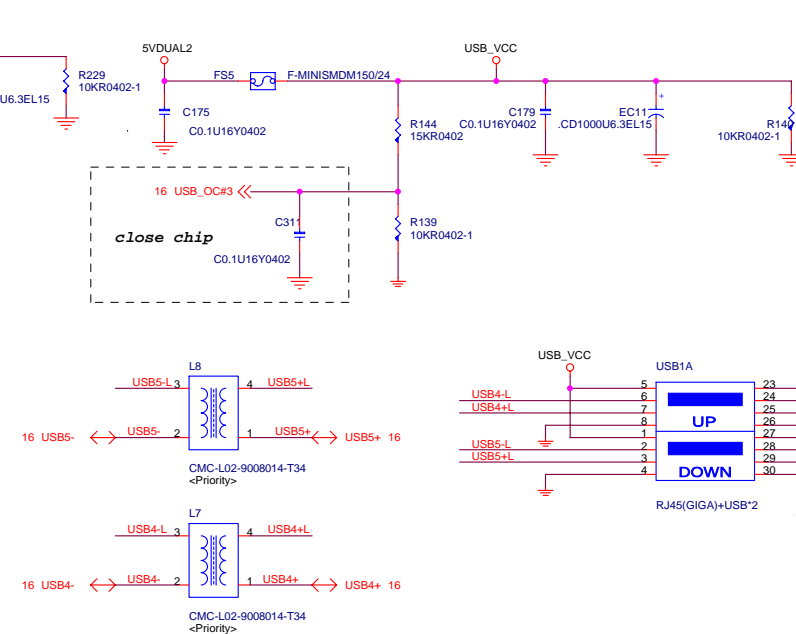
PCI1EXTENDER/PCI2		
Size	Document Number	Rev

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Date: Friday, March 31, 2006	Sheet 19 of 35	

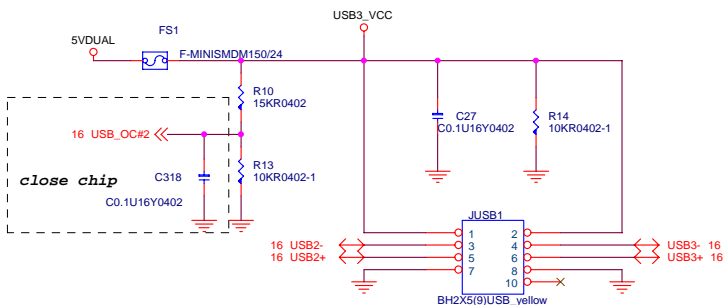
POWER CIRCUIT FOR USB PORT 6,7,8,9 (REAR)



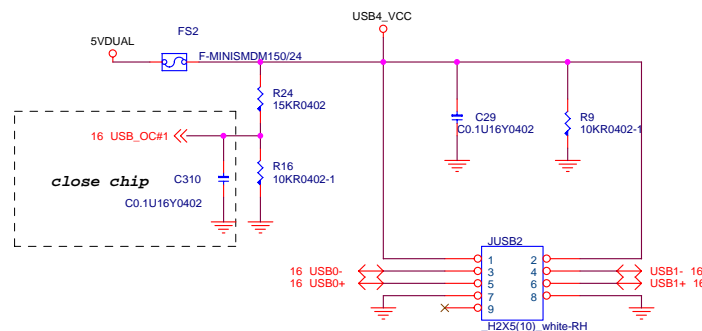
EXTERNAL USB PORT 4,5(REAR)



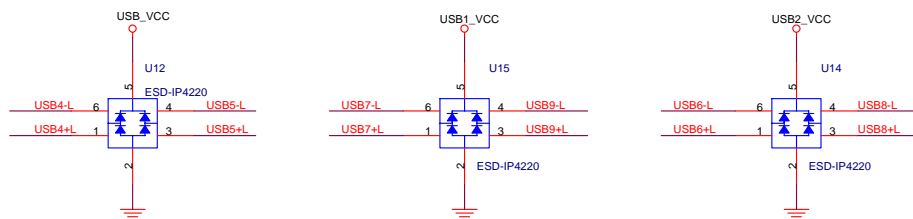
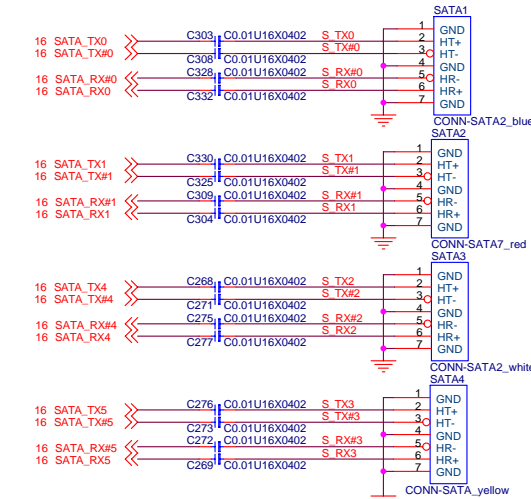
EXTERNAL USB PORT 2,3



EXTERNAL USB PORT 0,1

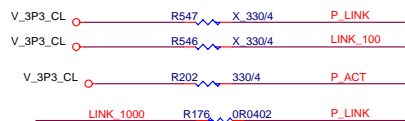
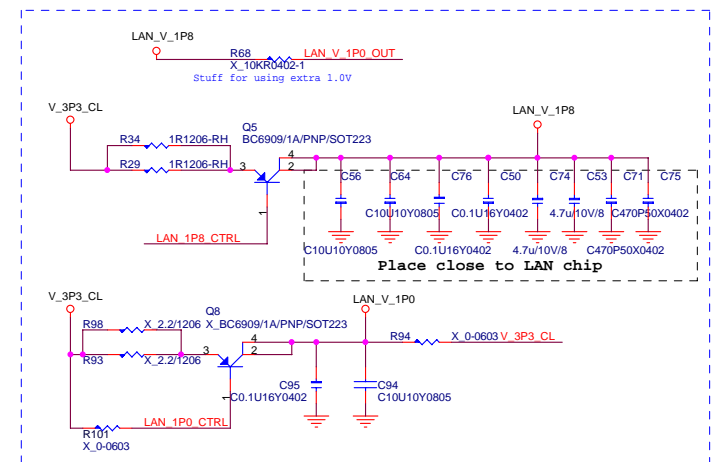
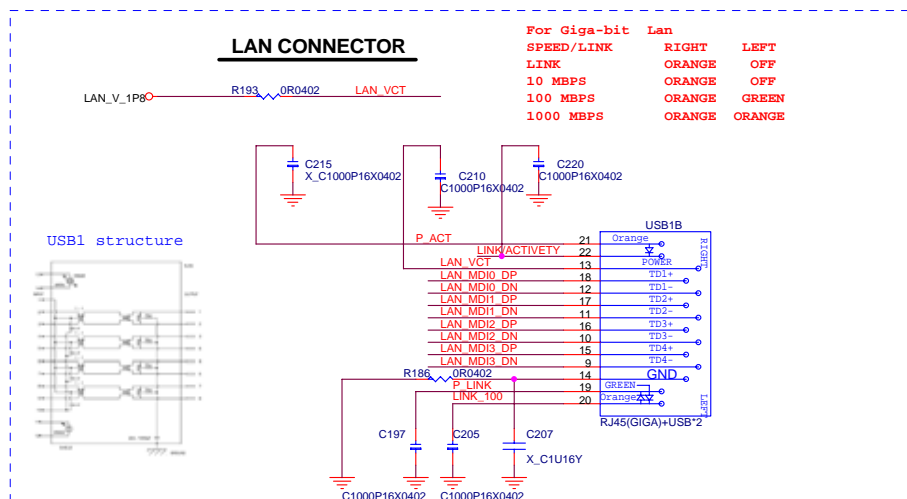
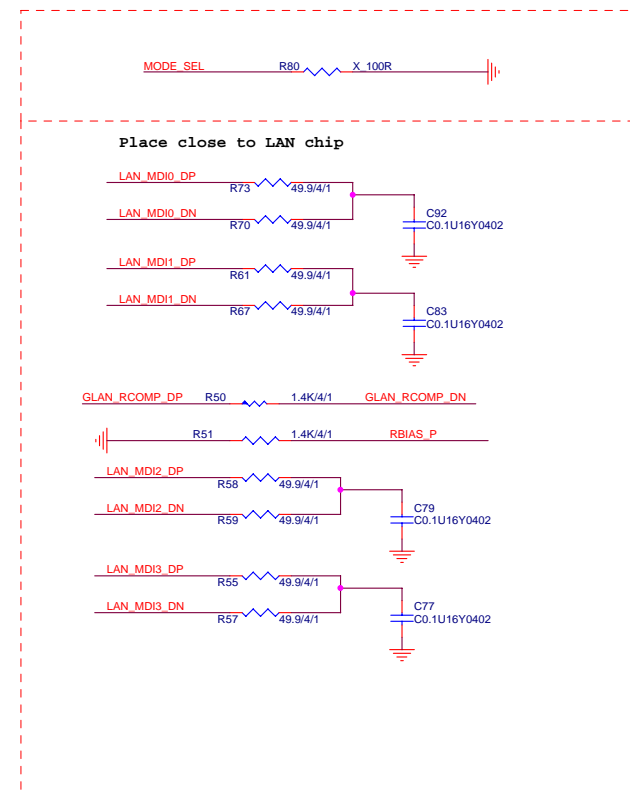
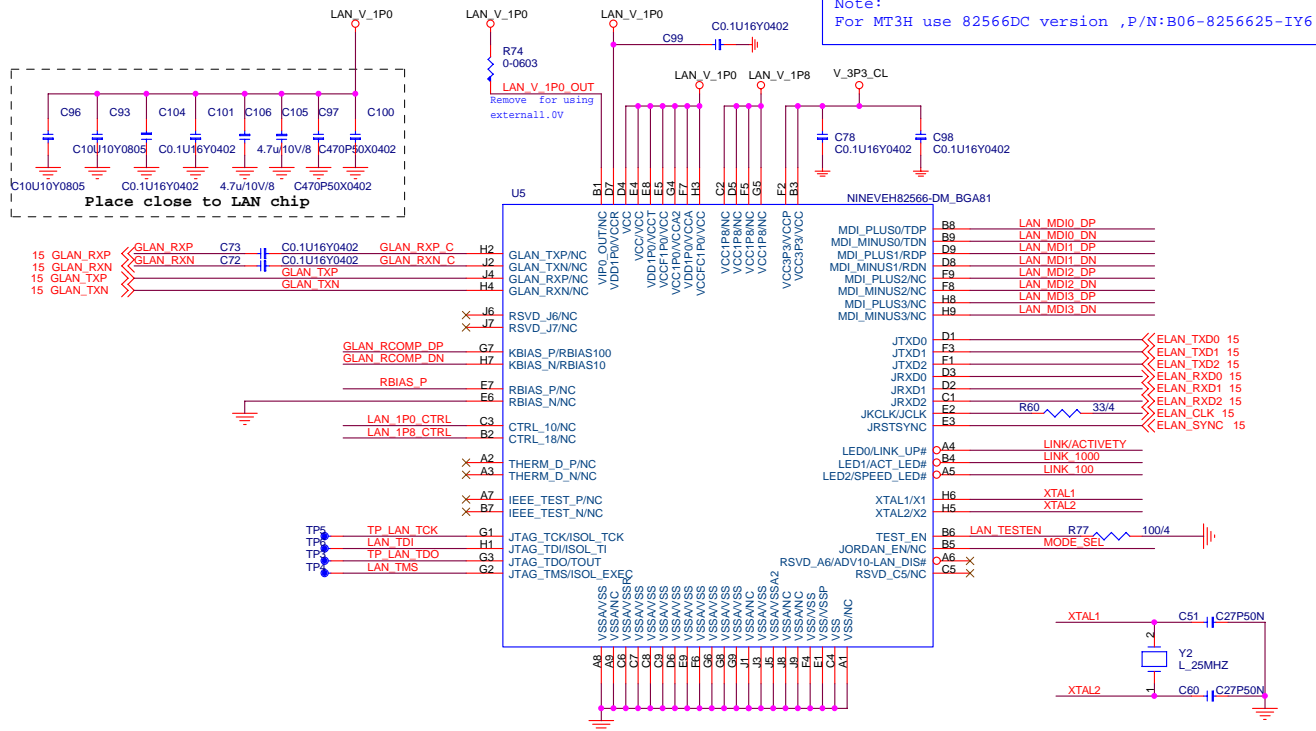


SERIAL ATA CONNECTOR BLOCK

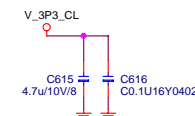



For EMI reserve
VCC5
C341
C1000P16X0402
Please close SATA2 connector

LAN - NINEVEH

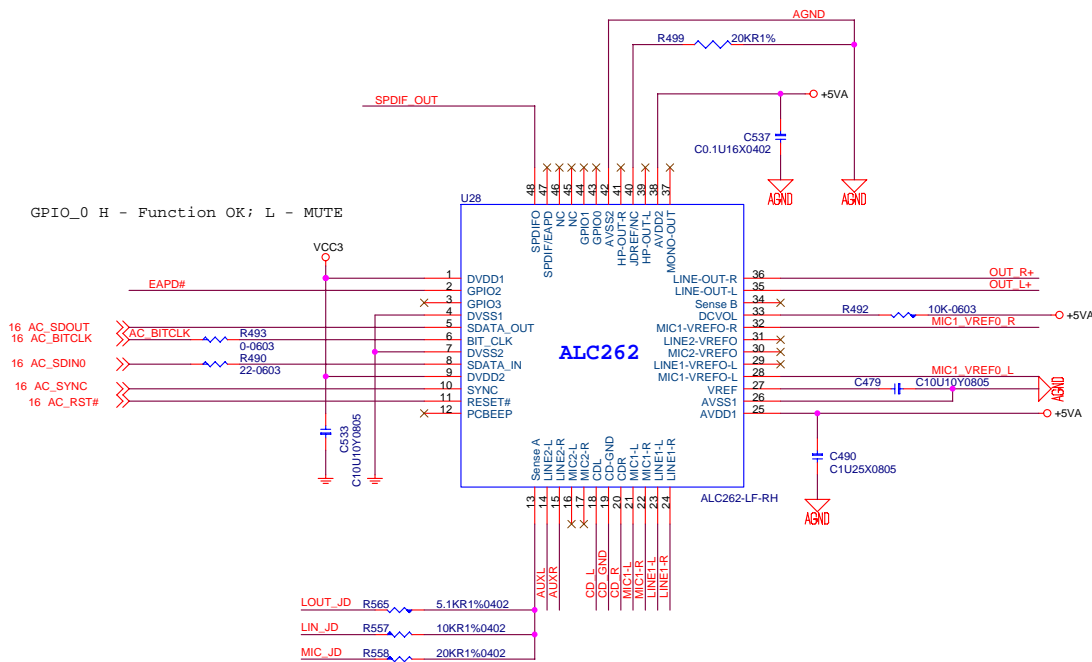


ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW WOL DIS-->HIGH

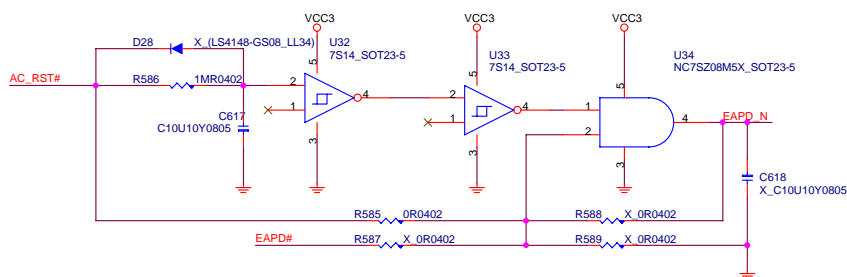


 MICRO-START INTL CO.,LTD.			
Title			
LAN-NINEVEH 82566DM			
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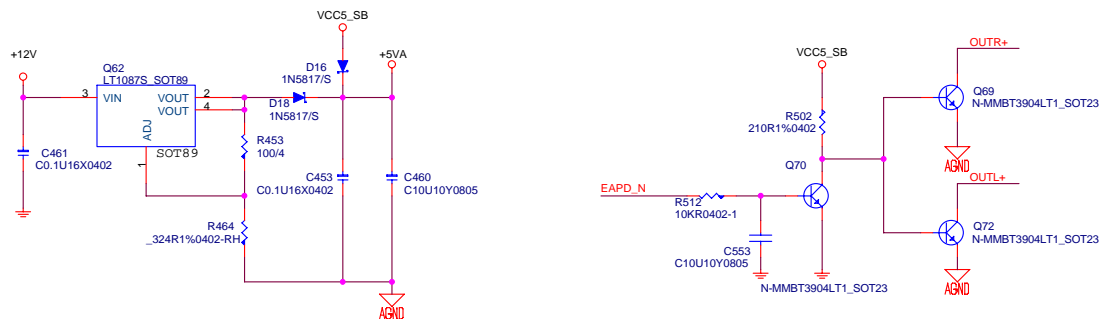
GPIO_0 H - Function OK; L - MUTE



POP noise circuit

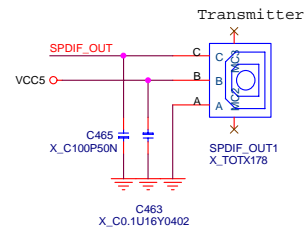


AUDIO CODE REGULATORS



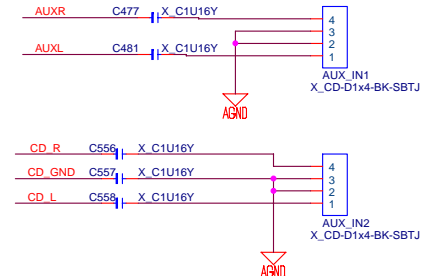
SPDIF OUT

Note:
For MT3H stuff



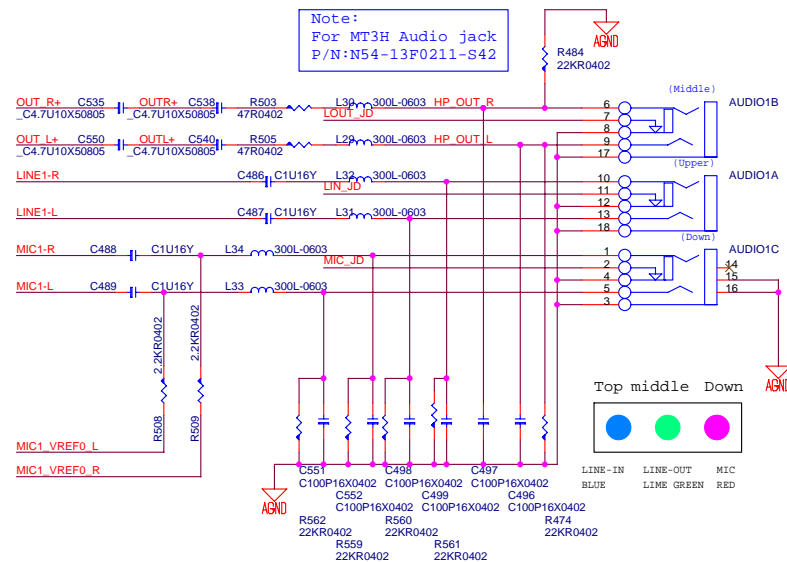
AUX IN

Note:
For MT3H stuff

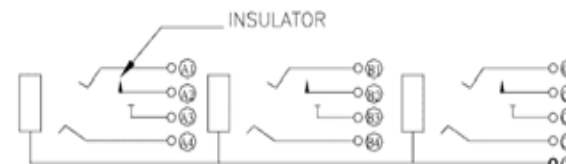


PHONE JACK.

Note:
For MT3H Audio jack
P/N:N54-13F0211-S42

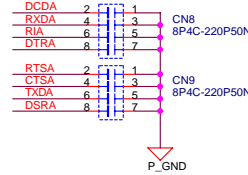
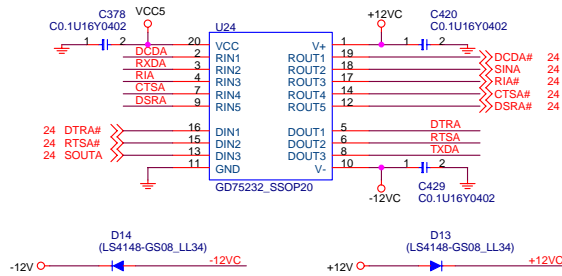


Jack schematic:



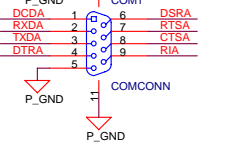
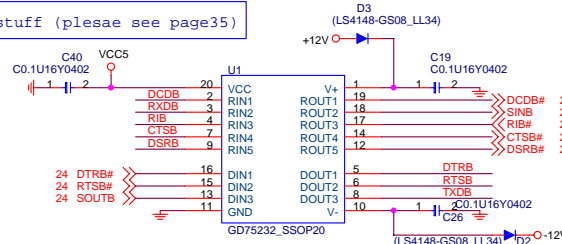
C1→5, C2→4, C3→2, C4→1
B1→9, B2→8, B3→7, B4→6
A1→13, A2→12, A3→11, A4→10
C0→3, 15, 16, 17, 18
Prevent function→14
C→ MIC, B→Line out, A→Line in

SERIAL PORT 1

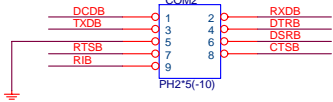


SERIAL PORT 2

Note:MT3H unstuff (plesae see page35)

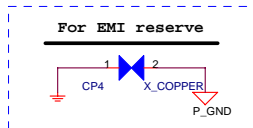
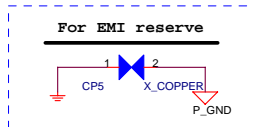


COM2 HEADER

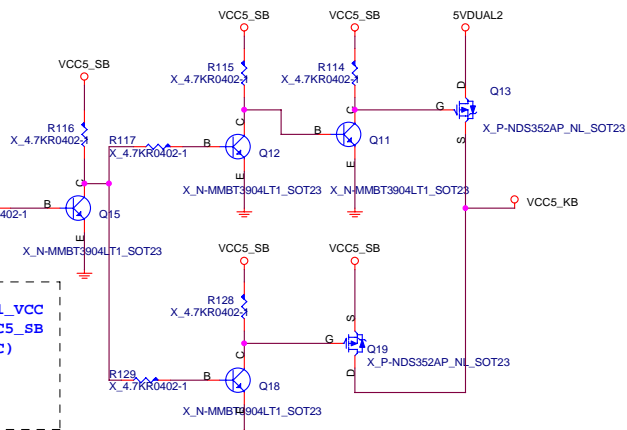


K/B Power supply function for NEC

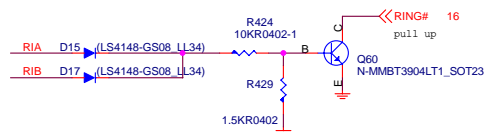
Note:MT3H stuff (plesae see page35)



GPIO_KB
HI:VCC5_KB = USB1_VCC
LOW:VCC5_KB = VCC5_SB
VCC_DUAL(USB1_VCC)
S0/S1:VCC5
S3:VCC5_SB
S4/S5:0V

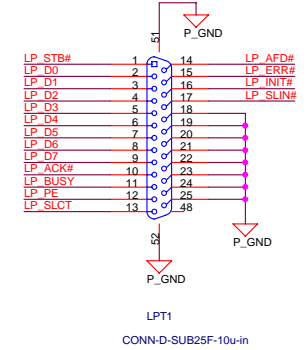
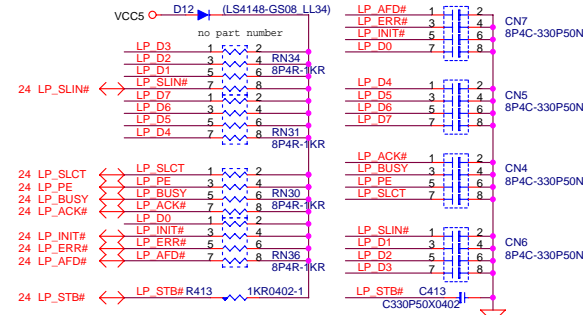


Wake On Modem Header

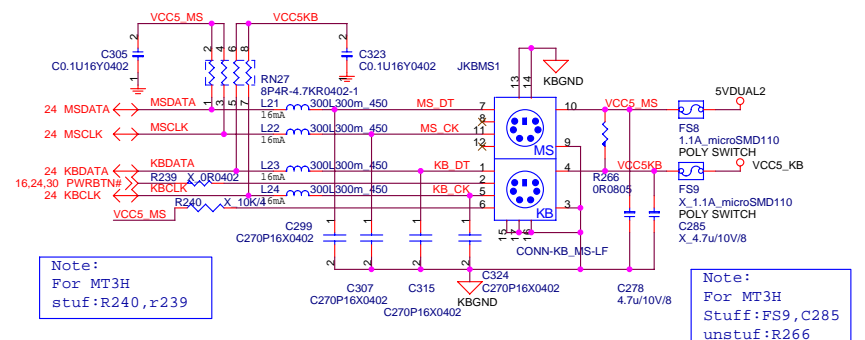


PARALLAL PORT

24 LP_D[0..7] ↔ LP_D[0..7]

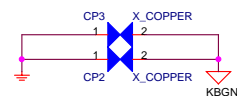


PS2 KEYBOARD & MOUSE CONNECTOR

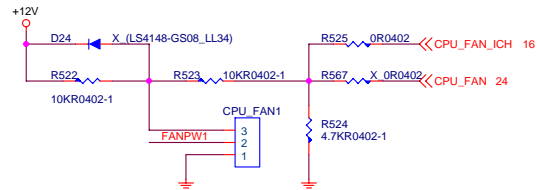
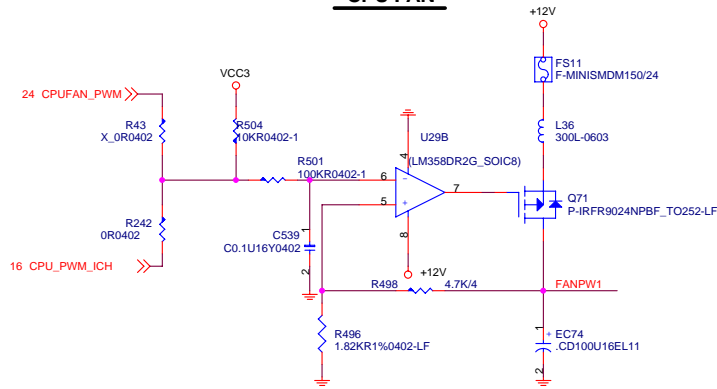


Note:
For MT3H
stuff:R240,r239

Note:
For MT3H
Stuff:FS9,C285
unstuf:R266



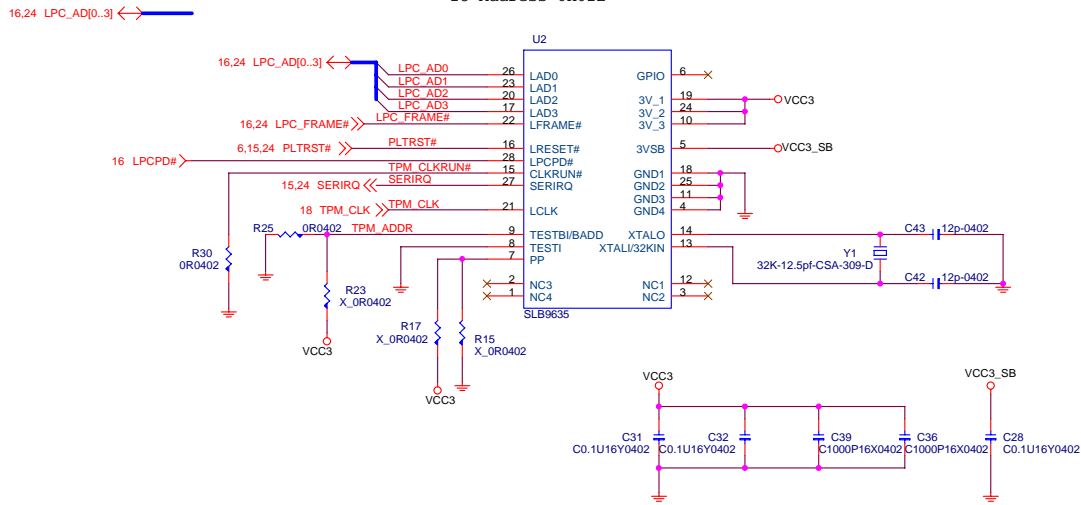
CPU FAN



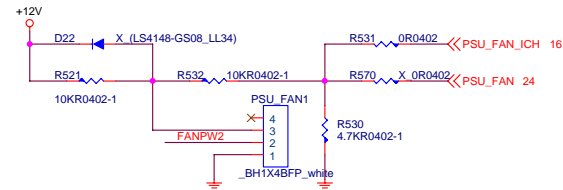
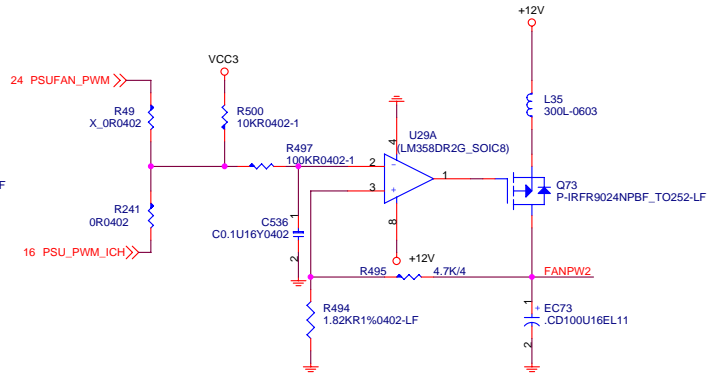
TPM 1.2

Note: MT3H unstuff (plesae see page35)

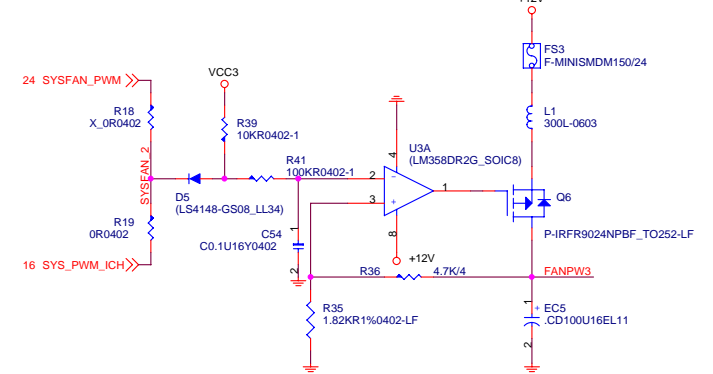
IO Address: 0x02E



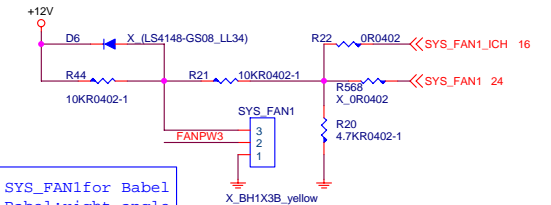
PSU FAN



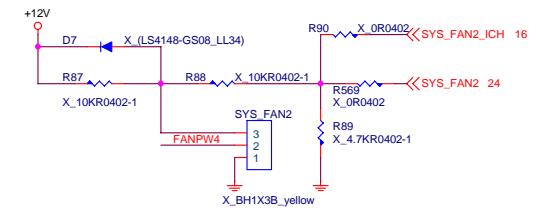
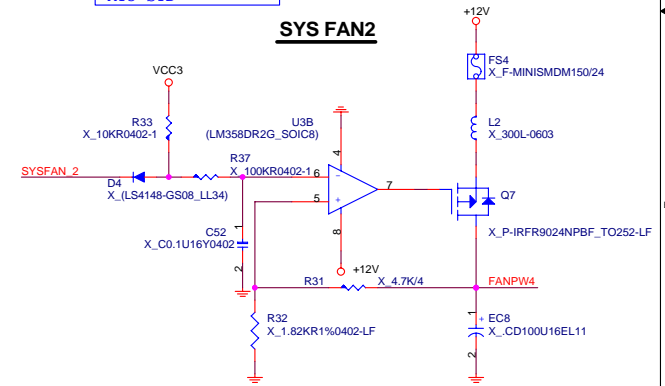
SYS FAN1



SYS_FAN1 for Babel
Babel: right angle
SYS_FAN2 for MT3H
MT3: STD



SYS FAN2



For EMI reserve

VCC5
C346 C0.1U16Y0402

Please close (-1905 -1465)

For EMI reserve

VCC5
C85 C0.1U16Y0402

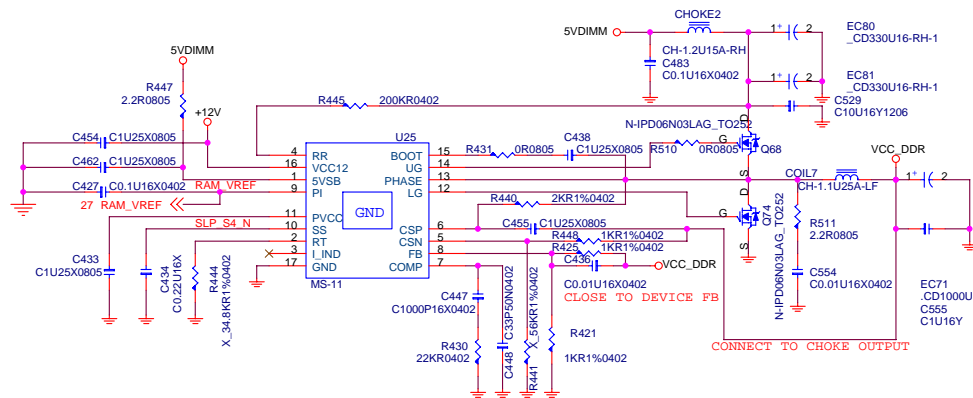
Please close (-2450 5020)



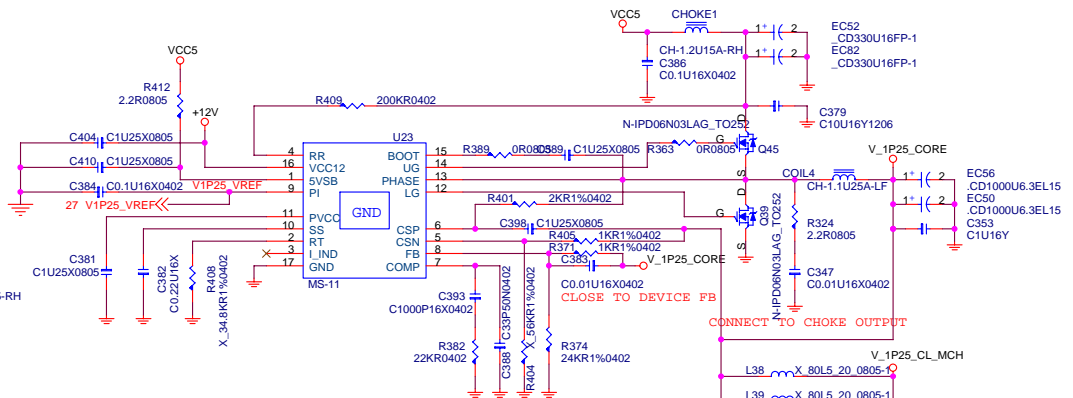
MICRO-START INTL CO.,LTD.

Title			FAN/TPM1.2
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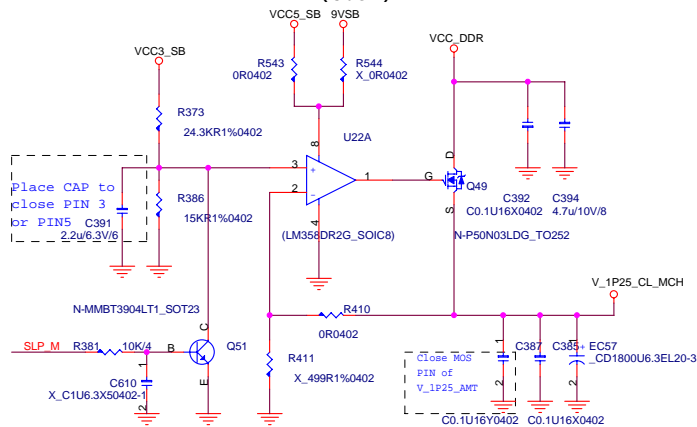
1.8V POWER
(25A)



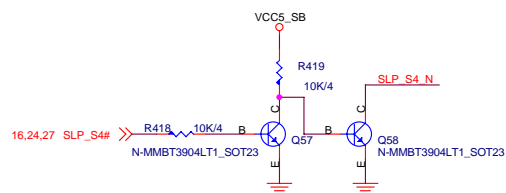
GMCH/ICH8 1.25V POWER
(21.3A)



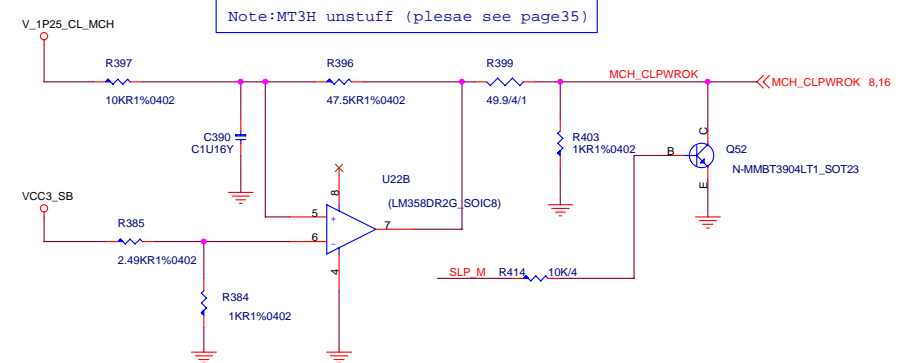
Note:for MT3H
Stuff L38,L39

$$\frac{V_{1P25_CL_MCH}}{(3.8A)}$$


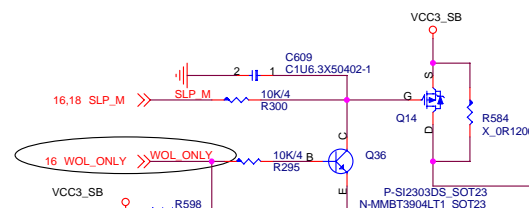
Note: MT3H unstuff (plesae see page35)



Note:MT3H unstuff (plesae see page35)



Note: MT3H unstuff (plesae see page35)

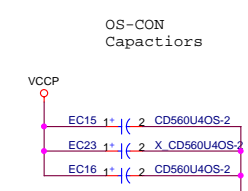
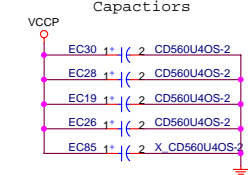
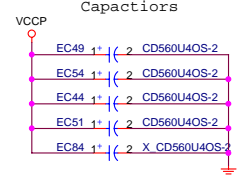
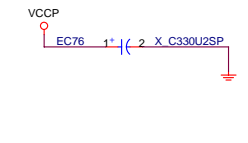
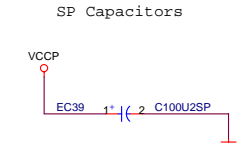
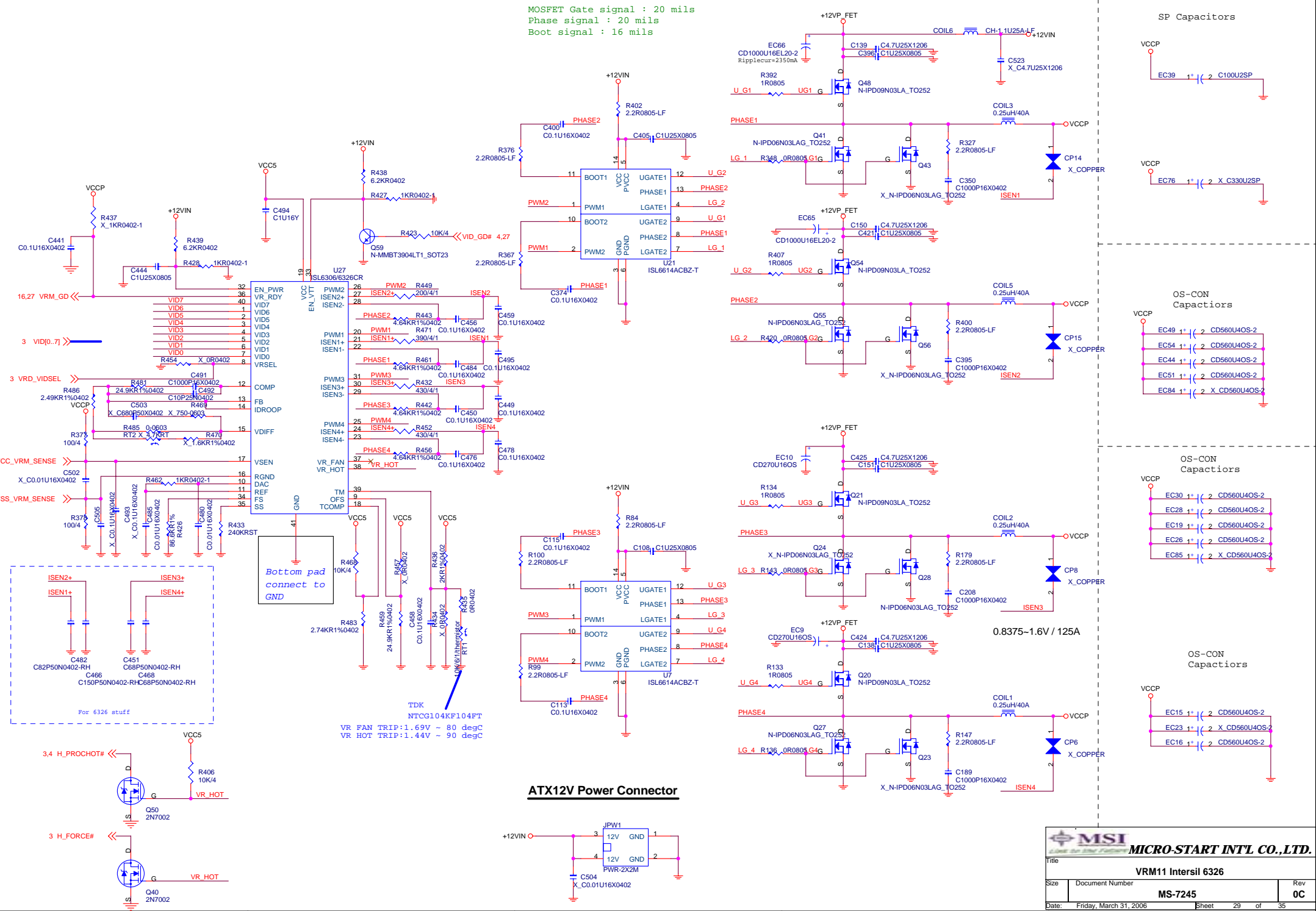
$$\frac{V_{3P3_CL}}{(711mA)}$$


For WOL ON
Stuff:R598

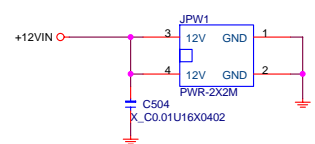
Note: MT3H unstuff (plesae see page35)


```
Note:
SLP_S4#
AMT Disable-->indicate ACPI S4 state,DRAM power off.
AMT Enable-->not be asserted ACPI S4 state,DRAM power ON
SLP_M#
AMT Enable SLP_M#-->Control the overall power to Intel
AMT during ACPI S3-S5.
S4_SATE#
AMT Enable-->indication of ACPI S4 state
```

MOSFET Gate signal : 20 mils
Phase signal : 20 mils
Boot signal : 16 mils



ATX12V Power Connector



**MICRO-START INTL CO.,LTD.**

Title VRM11 Intersil 6326		
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Front Panel

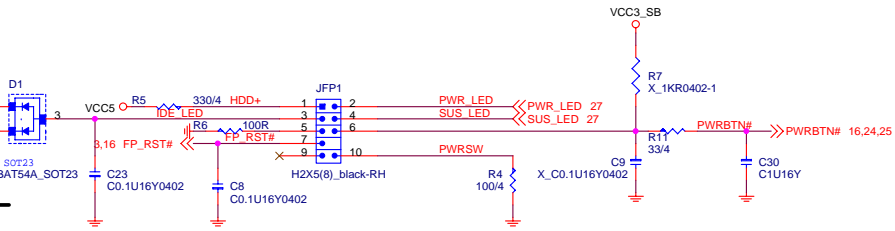
IDE LED

21 IDEACTP#
Active-low

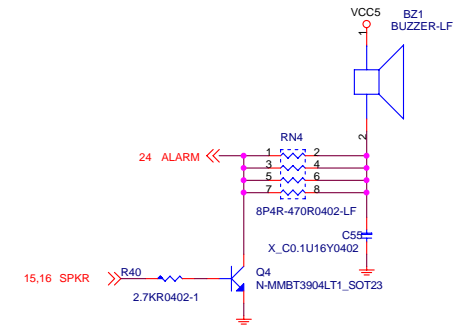
Active-low

SERIAL ATA LED

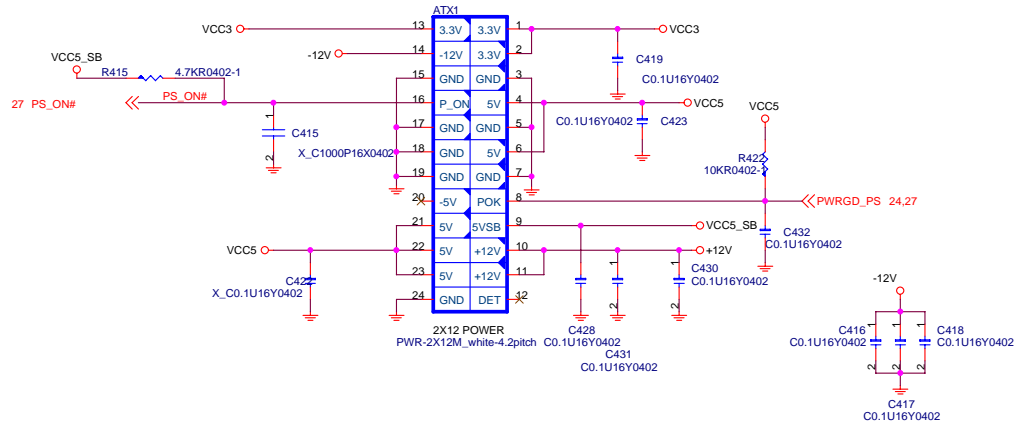
16 SATALED#



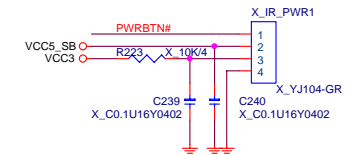
SPEAKER



ATX Connector



For NEC IR POWER



ICH8

GPIO Pin	Type	Default	Function	Power	MUXED/ UNMUXED	Pin-out
GPIO 0	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AF9
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AF5
GPIO 2	I/O	GPI	PIRQ#E pull-up to VCC3 with 10K	VCC3		D5
GPIO 3	I/O	GPI	PIRQ#F pull-up to VCC3 with 10K	VCC3		F10
GPIO 4	I/O	GPI	PIRQ#G pull-up to VCC3 with 10K	VCC3		G11
GPIO 5	I/O	GPI	PIRQ#H pull-up to VCC3 with 10K	VCC3		F9
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AE6
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AC8
GPIO 8	I/O	GPI	SIO_PME# connect to SIO,pull_up VCC3_SB with 10k	VCC3_SB	UNMUXED	AE16
GPIO 9	I/O	MGPIO3	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AG18
GPIO 10	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AF20
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		AF21
GPIO 12	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VBT	UNMUXED	AC19
GPIO 13	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	UNMUXED	AF18
GPIO 14	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AH24
GPIO 15	I/O	GPO	PCI_STOP	VCC3_SB	UNMUXED	AE21
GPIO 16	I/O	GPO	SIO HWM_INT,pull_up VCC3 with 10K(change to GPI)		UNMUXED	AE11
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AC7
GPIO 18	I/O	GPO	NC		UNMUXED	AC11
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AD8
GPIO 20	I/O	GPO	NC		UNMUXED	AG8
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AB11
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AE7
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull_up VCC3 with 10K	VCC3	MUXED	C3
GPIO 24	I/O	GPO	NC		MUXED	AG23
GPIO 25	I/O	GPO	CPU_STOP	3.3V_SB	UNMUXED	AH17
GPIO 26	I/O	GPO	S4 STATE			AH25
GPIO 27	I/O	GPO	NC	3.3V_SB		AD20
GPIO 28	I/O	GPO	NC			AD15
GPIO 29	I/O	OC5#	OC#3 connect to USB connector	3.3V_SB		AE15
GPIO 30	I/O	OC6#	OC#4 connect to USB connector	3.3V_SB		AG13
GPIO 31	I/O	OC7#	OC#4 connect to USB connector	3.3V_SB		AF14
GPIO 32	I/O	GPO	SIO_SMI# connect to SIO,pull up VCC3 with 10k	VCC3	UNMUXED	AH7
GPIO 33	I/O	GPO	Pull-up to VCC3 with 8.2K		UNMUXED	AG7
GPIO 34	I/O	GPO	NC		UNMUXED	AG12
GPIO 35	I/O	GPO	NC			AD12
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF8
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AD9
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AH6
GPIO 39	I/O	GPI	Pull-down to GND with 10K directly	VCC3		AC10
GPIO 40	I/O	OC1#	OC#1 connect to USB connector	VCC3		AH14
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	VCC3		AG14
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	VCC3		AG15
GPIO 43	I/O	OC4#	OC#3 connect to USB connector	VCC3		AH15
GPIO 48	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF7
GPIO 49	I/O	CPU_PWRGD	H_PWRGD connect to CPU	VTT_OUT		AF25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 10K	VCC5	MUXED	C16
GPIO 51	I/O	GNT1#	GNT1#		MUXED	A15
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC5 with 10K	VCC5	MUXED	B16
GPIO 53	I/O	GNT2#	GNT2#		MUXED	D17
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 10K	VCC5	MUXED	A9
GPIO 55	I/O	GNT3#	GNT3#		MUXED	B9

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI1 EXTENT	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK1
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK0
VT6410	PIRQ#E	PREQ#2 PGNT#2	AD20	RAIDCLK
PCI3	RESERVED	PREQ#3 PGNT#3	AD18	PCI_CLK3

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	SCLK_A0/SCLK_A0# SCLK_A1/SCLK_A1# SCLK_A2/SCLK_A2#
DIMM 2	0A2H	SCLK_A3/SCLK_A3# SCLK_A4/SCLK_A4# SCLK_A5/SCLK_A5#
DIMM 3	0A4H	SCLK_B0/SCLK_B0# SCLK_B2/SCLK_B2#
DIMM 4	0A6H	SCLK_B3/SCLK_B3# SCLK_B4/SCLK_B4# SCLK_B5/SCLK_B5#

SIO SCH5017


PIN NAME	PIN#	USAGE	Input/Output
GP43	92	GPIO_KB	OUTPUT
GP27	36	SIO_SMI#	OUTPUT
GP42	90	SIO_PME#	OUTPUT
GP61	93	CLEAR_PASSWORD	INPUT

SMBus DISTRIBUTION

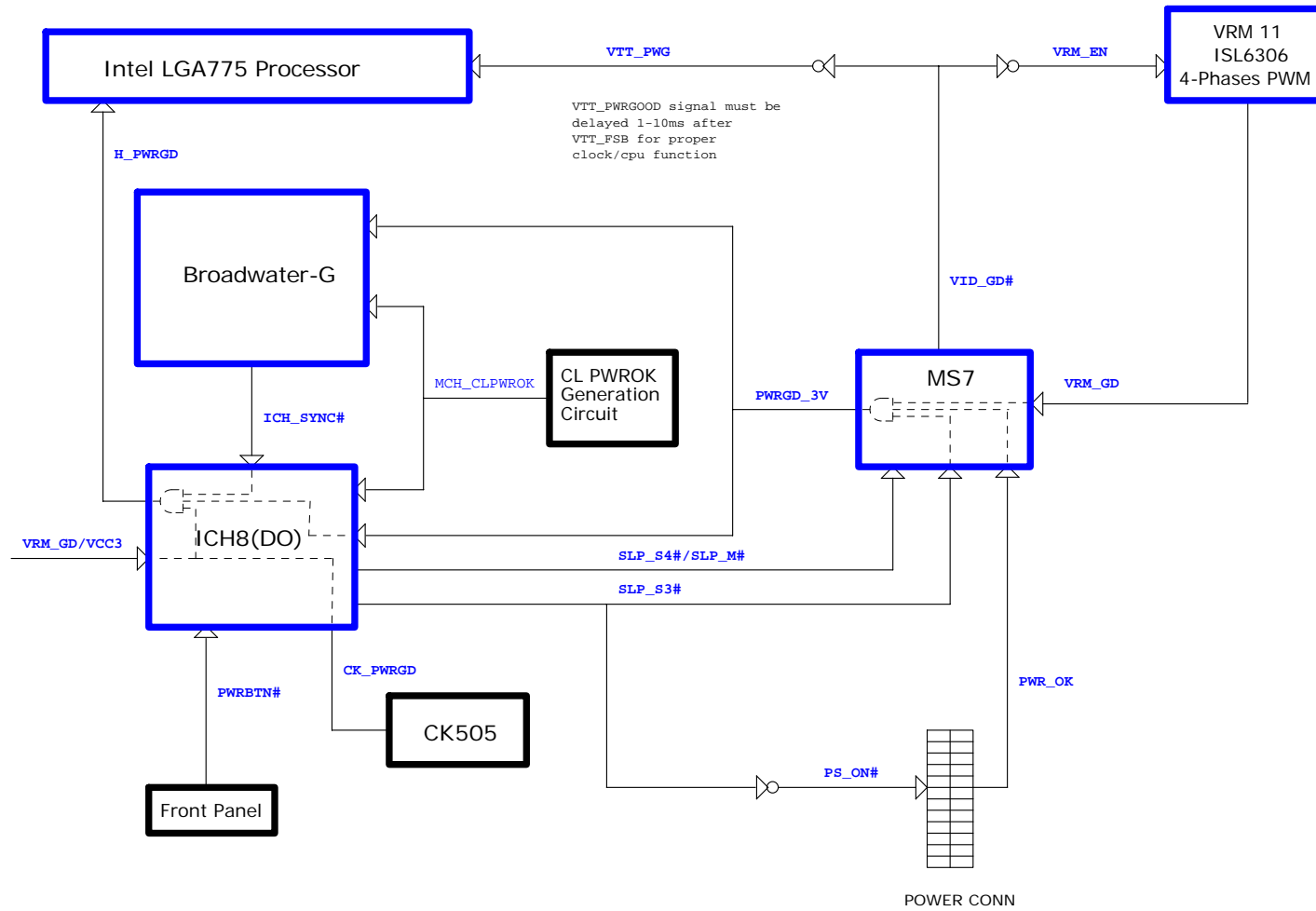
SMBus	Power	Load
SMBCLK	VCC3_SB	ICH8, SIO,PCI EXPRESS x16,x1
SMBCLK_ISO	VCC3	DIMM, CLK GEN, SIO, MS7,LAN

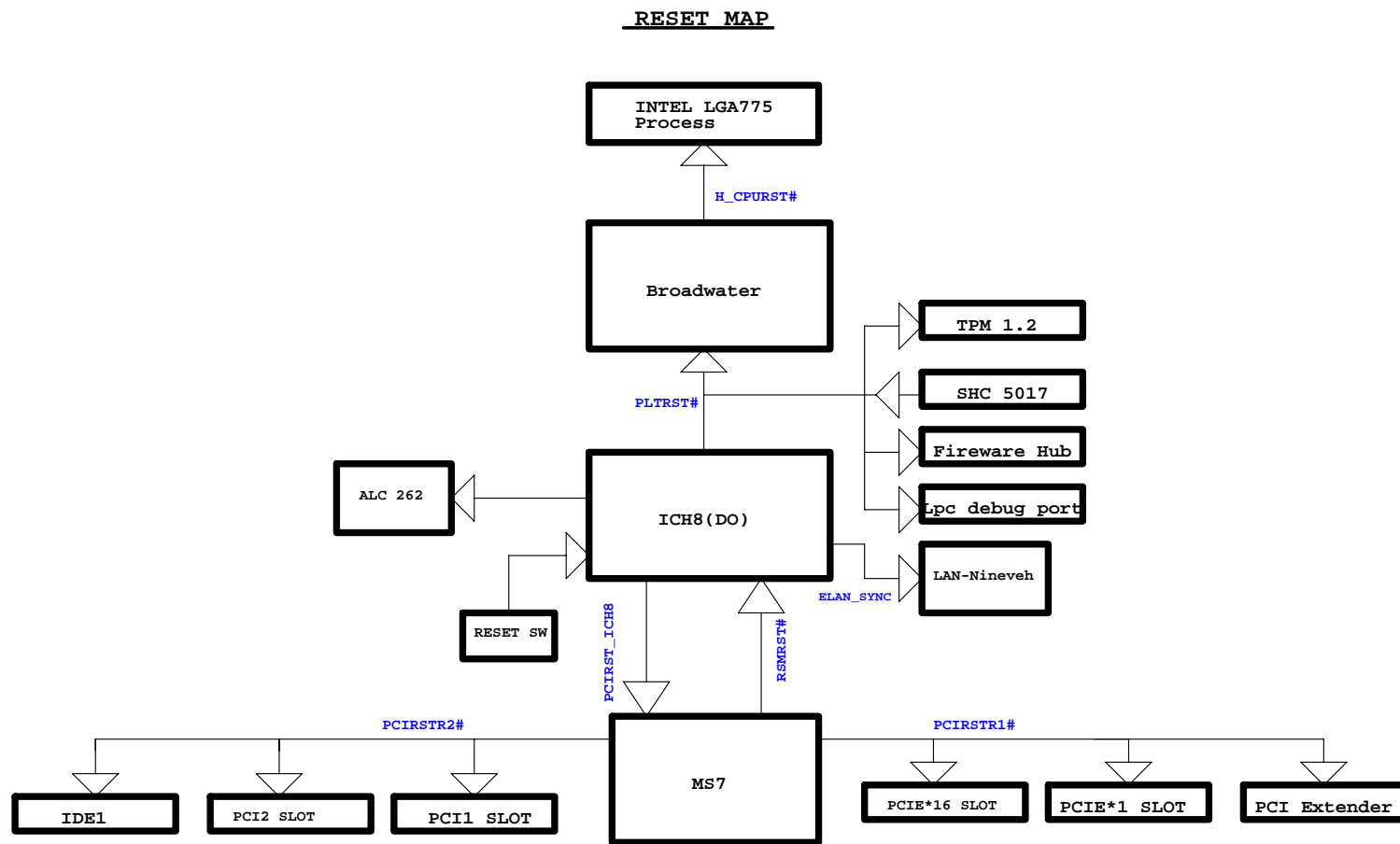
JUMPER SETTING

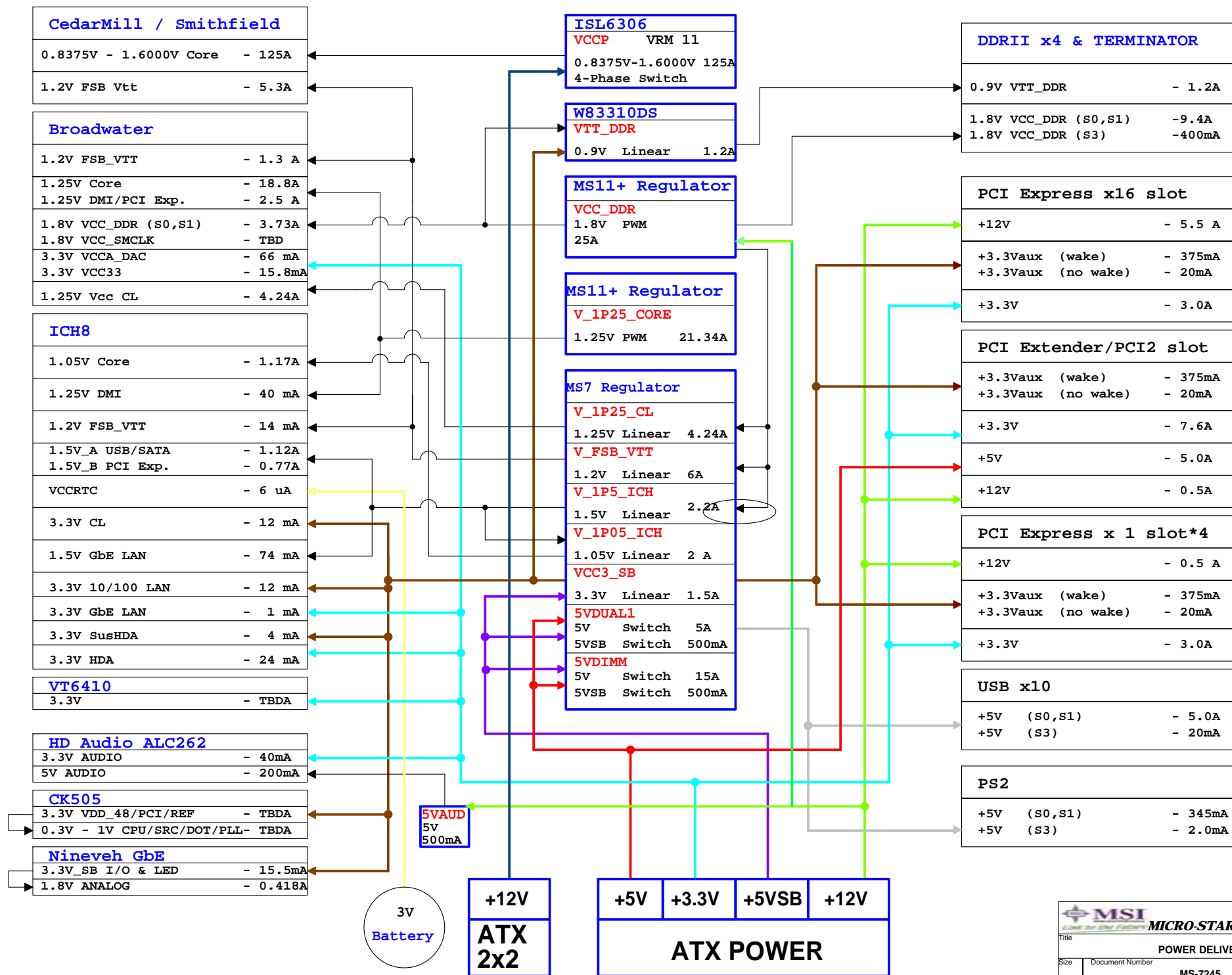
JBAT1	(1-2)Normal	(2-3)Clear
INTRUDER	Short Normal	Open warning
JPWD1	(1-2) open clear	(1-2)short Normal

 MICRO-START INTL CO.,LTD.		
Title		
GPIO PIN definition		
Size	Document Number	Rev
	MS-7245	0C
Date:	Friday, March 31, 2006	Sheet 31 of 35

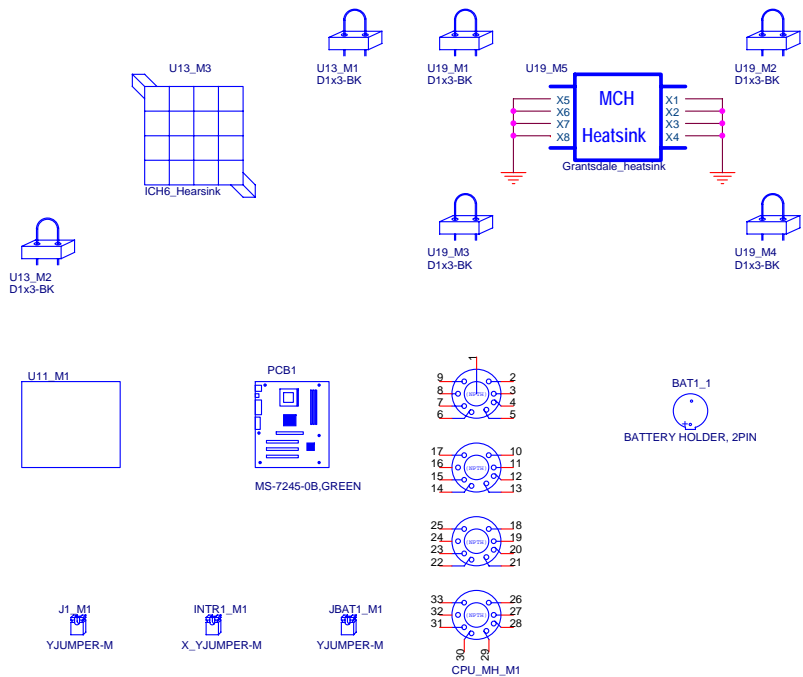
PWROK MAP



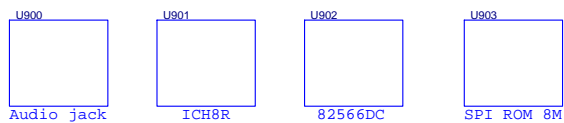




COMMON MANUAL PART



MT3H MANUAL PART



For MT3H BOM

1.For MT3H Audio jack P/N:N54-13F0211-S42

2.Remove TPM1.2

Unstuff:

U2,R30,R25,C43,C42,Y1,C31,C32,C39,C36,C28,R102

3.None AMT function

Stuff:

R113,R205,R572,R584,L38,L39

Unstuff:

R124,Q33,R397,C390,R396,R399,

R403,Q52,R414,U22,R385,R384,R373,C391,R386,R543,R599,R381,Q51,R410,Q49,C392,C394,C387,C385,

EC57,R418,R419,Q57,Q58,C609,R300,Q36,R295,Q14

R198,Q30,R204,C216,R138,R142

4.Addition SPDIF function

Stuff:

SPDIF_OUT1,C465,C463

5.Change ICH8DO to ICH8R(OB1-ICH8R05-IY6)

6.Change Nineveh 82566DM to 82566DC (B06-8256625-IY6)

7.Addition keyboard power on function

Stuff:

R130,R116,Q15,R117,R129,R115,Q12,Q11,R128,Q18,R114,Q19,Q13,FS9,C285,R239,R240

Unstuff:

R266

8.Addition AUX*2

Stuff:

C477,C481,C556,C557,C558,AUX_IN1,AUX_IN2

9.Remove INTRUDER

unstuff:R3,INTR1

10.Change SPI flasf rom from 16M to 8M(M31-VF08003-S20)

11.Remove serial port2

Unstuff:

Com2,CN2,CN1,D3,C19,D2,U1,C40,C26

12.SYS_FAN2 for MT3H

Stuff:D4,R33,R37,R31,R32,C52,FS4,L2,Q7,EC8,R87,R88,R90,R89,SYS_FAN2

Unstuff:R22,R20,R21,R44,SYS_FAN1,EC5,Q6,L1,FS3,R36,R35,C54,R41,R39,D5